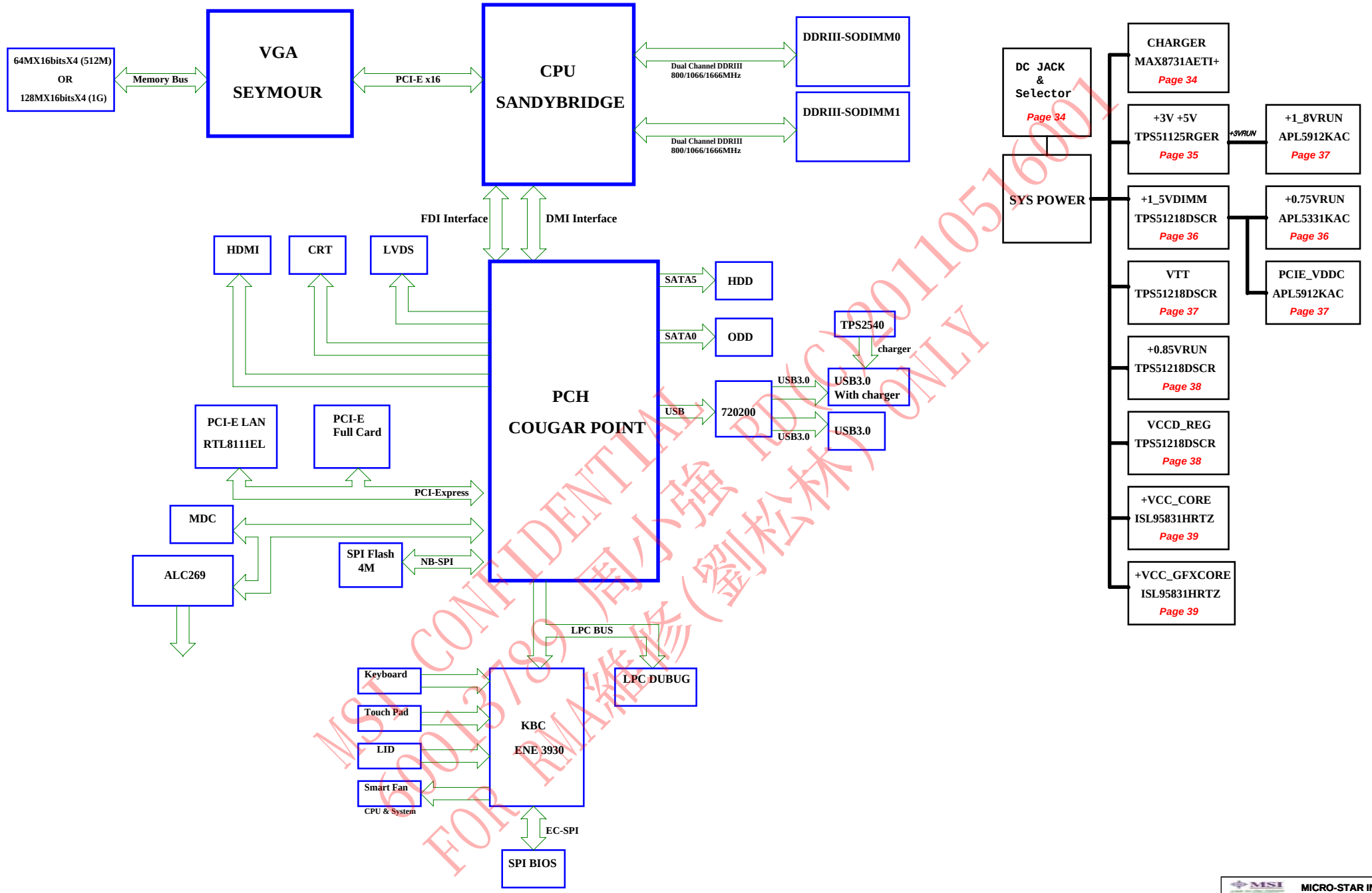

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Title

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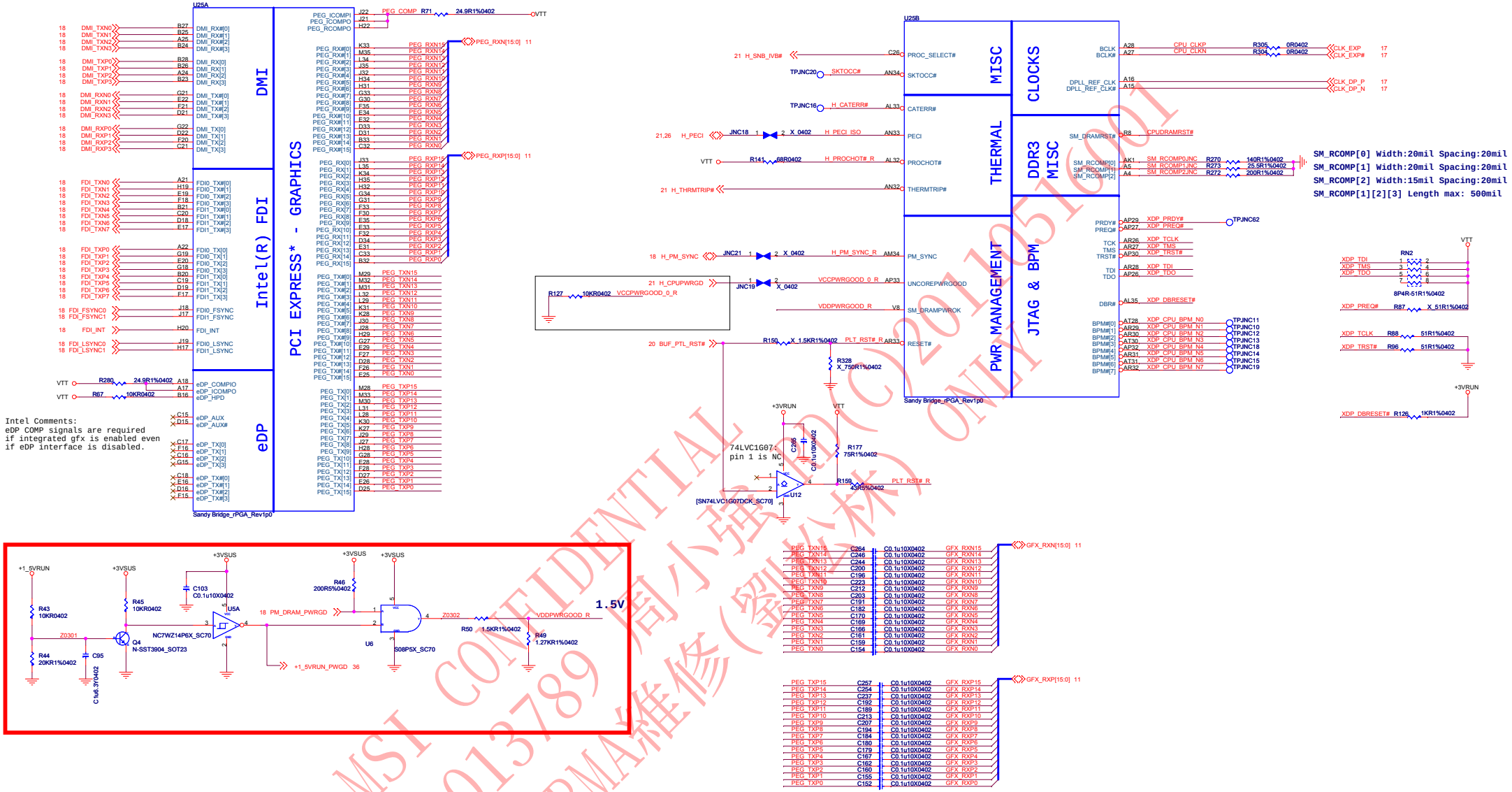
SANDYBRIDGE PROCESSOR (CLK,MISC,JTAG)



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MICRO-STAR INT'L CO.,LTD.			
Title: Processor			
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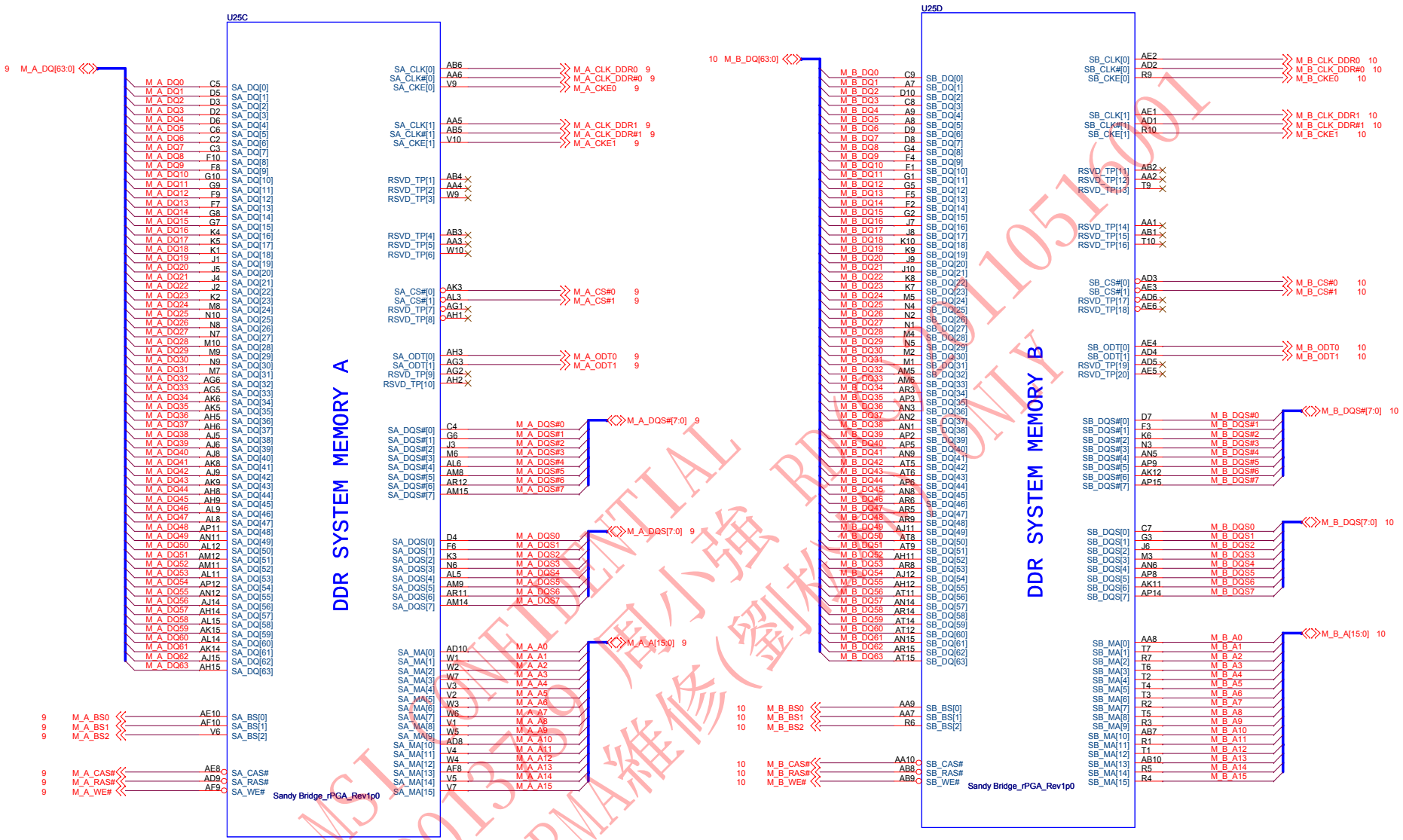
SANDYBRIDGE PROCESSOR (DDR3)



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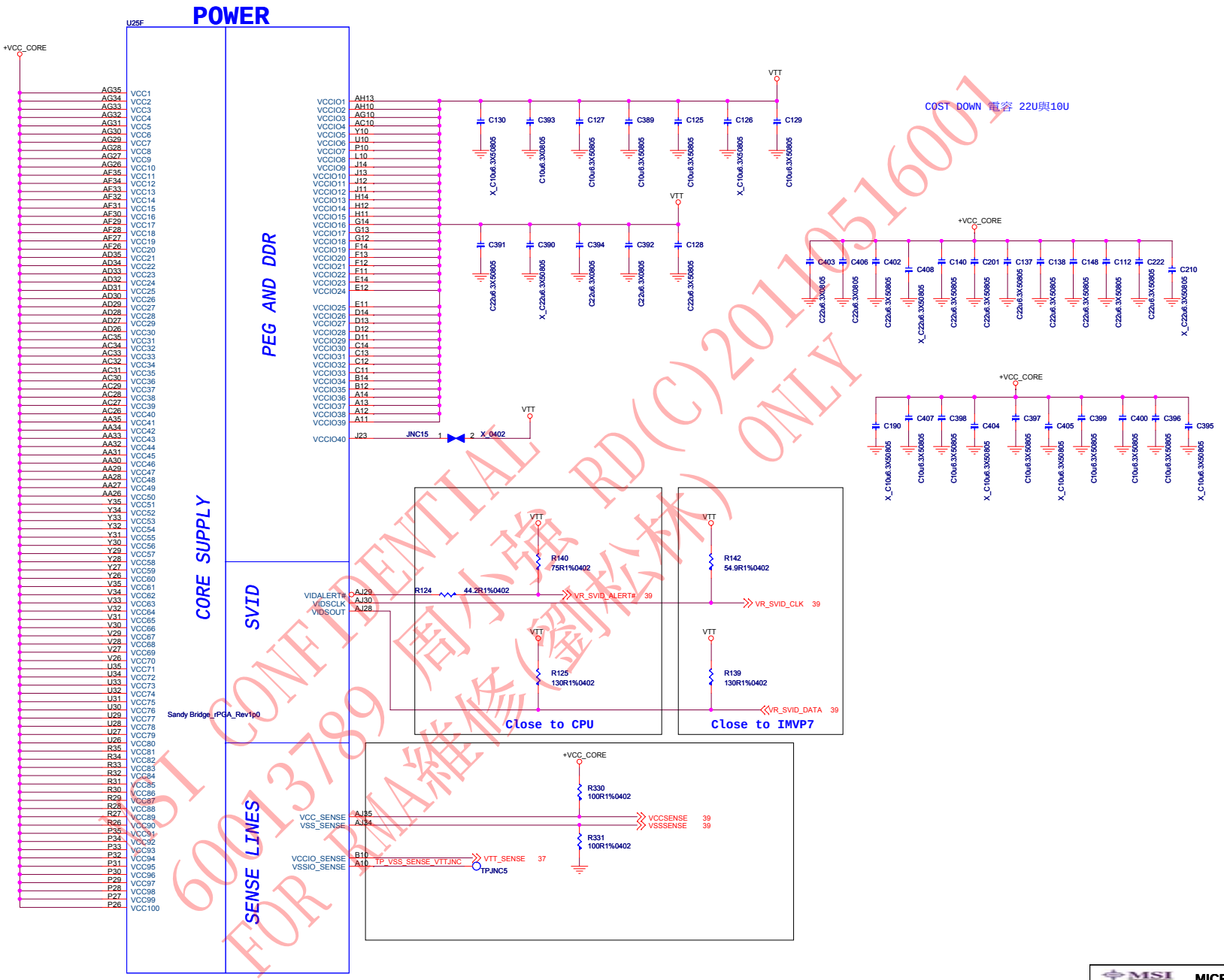
SANDYBRIDGE PROCESSOR (POWER)



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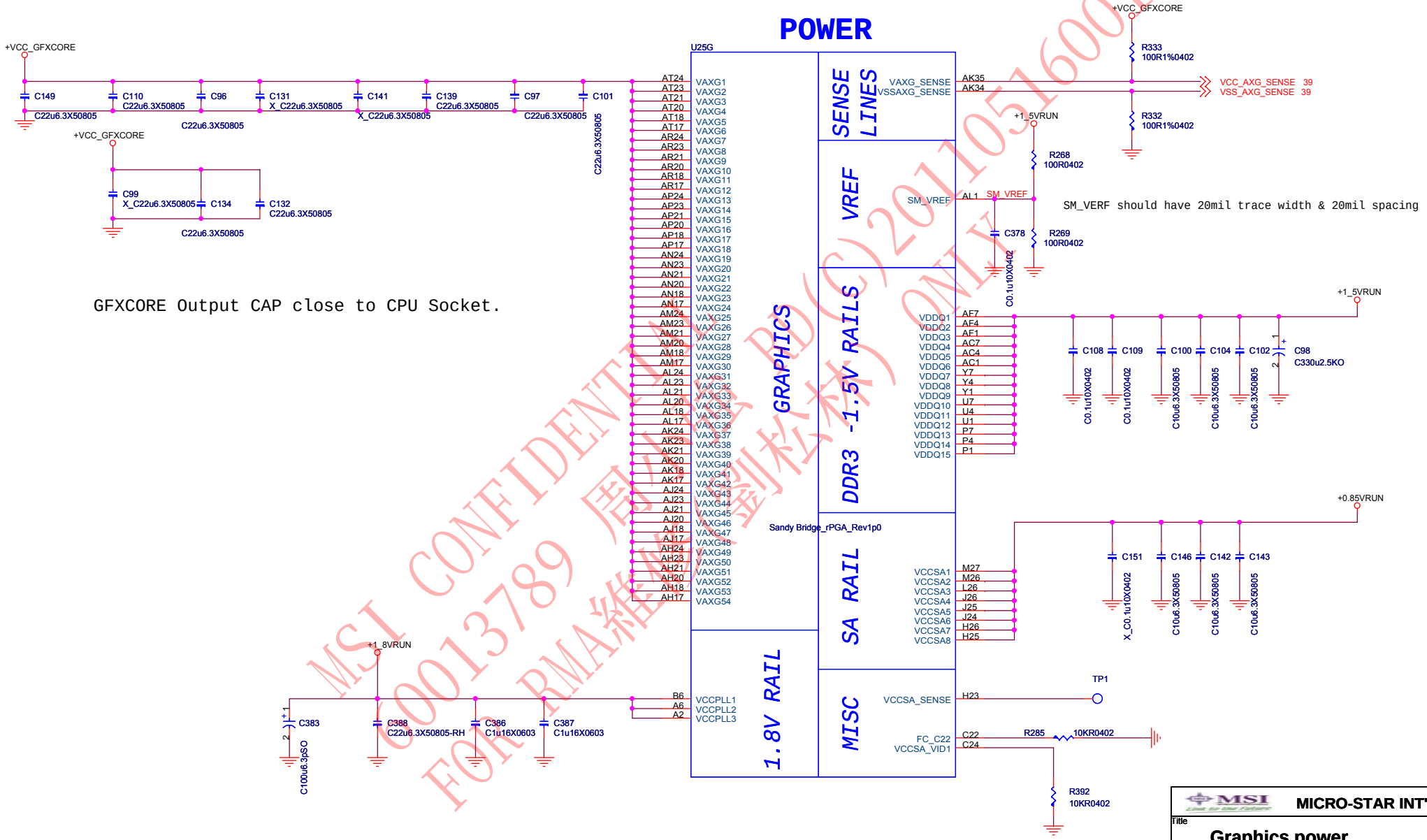
SANDYBRIDGE PROCESSOR (GRAPHICS POWER)



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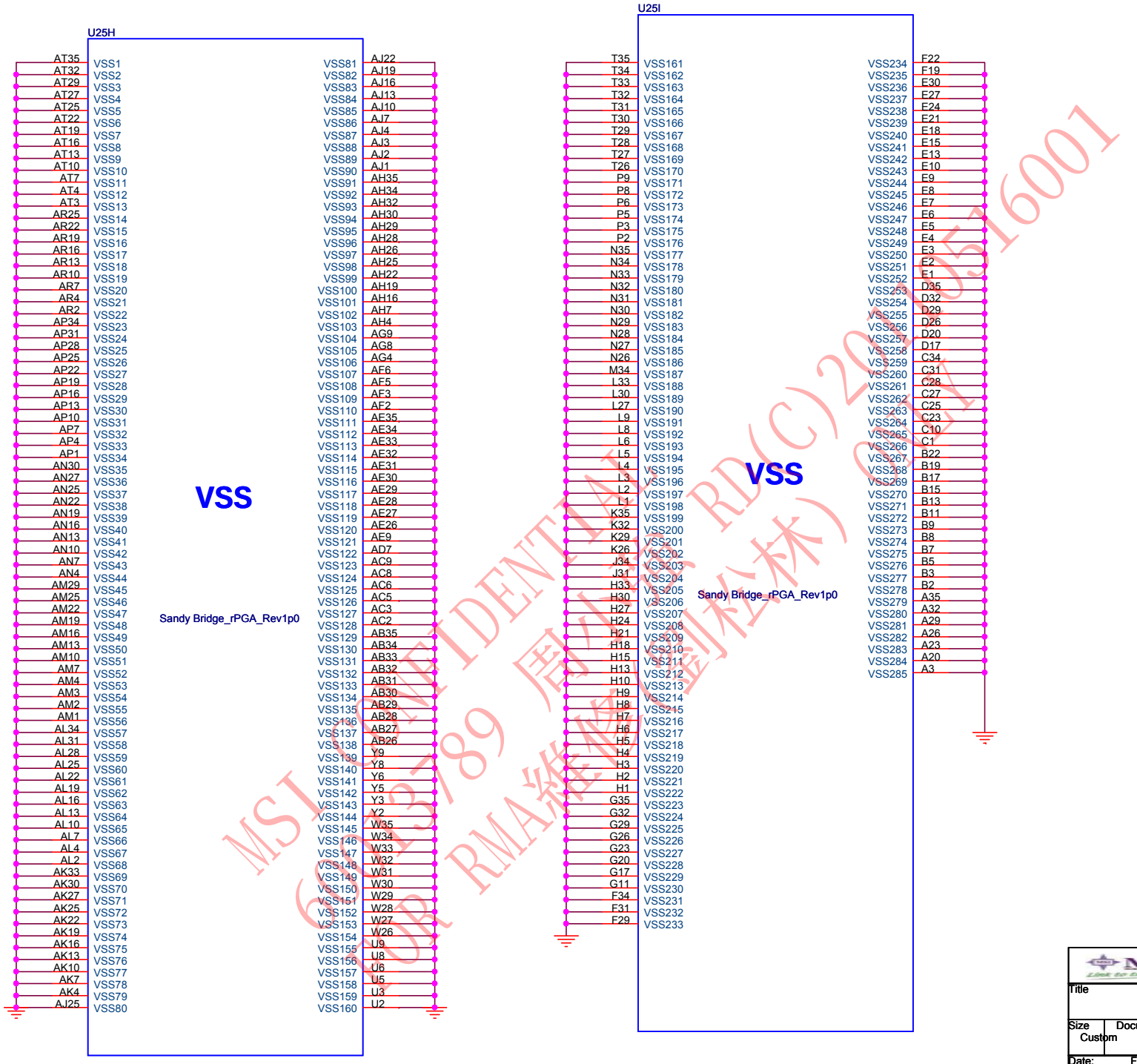
SANDYBRIDGE PROCESSOR (GND)



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Title	GND		
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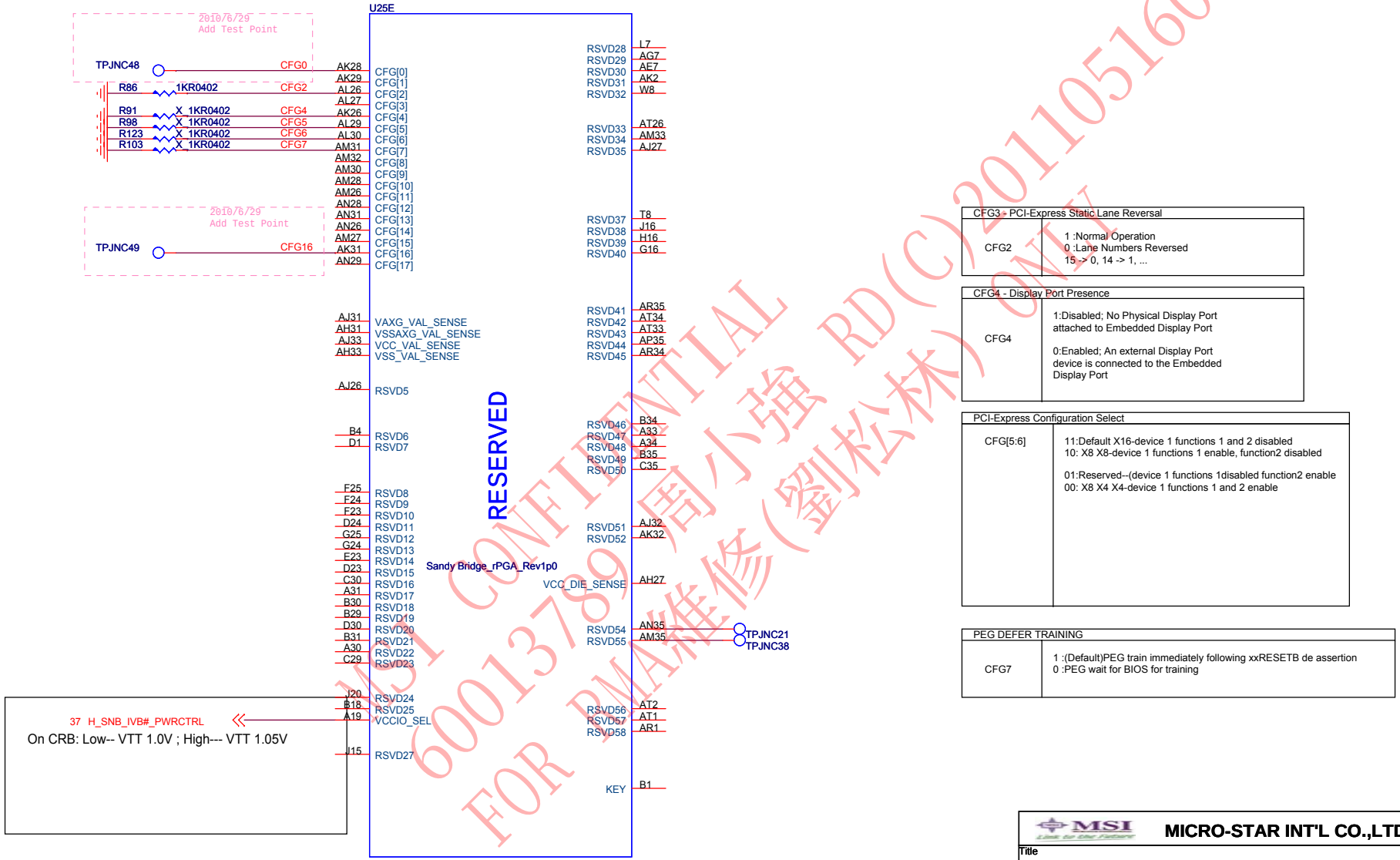
SANDYBRIDGE PROCESSOR (RESERVED)



CFG3 - PCI-Express Static Lane Reversal	
CFG2	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

PCI-Express Configuration Select	
CFG[5:6]	11:Default X16-device 1 functions 1 and 2 disabled 10: X8 X8-device 1 functions 1 enable, function2 disabled 01:Reserved--(device 1 functions 1disabled function2 enable 00: X8 X4 X4-device 1 functions 1 and 2 enable

PEG DEFER TRAINING	
CFG7	1 :(Default)PEG train immediately following xxRESETB de assertion 0 :PEG wait for BIOS for training

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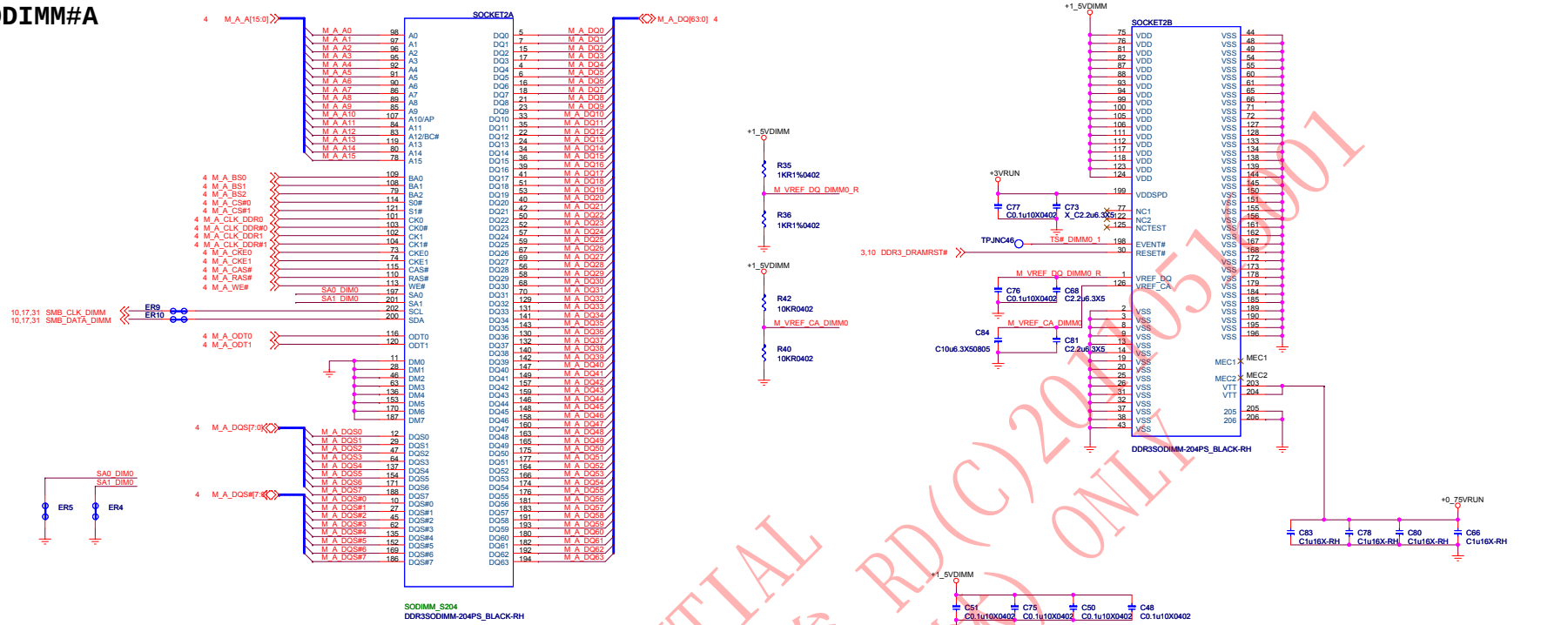
SODIMM#A

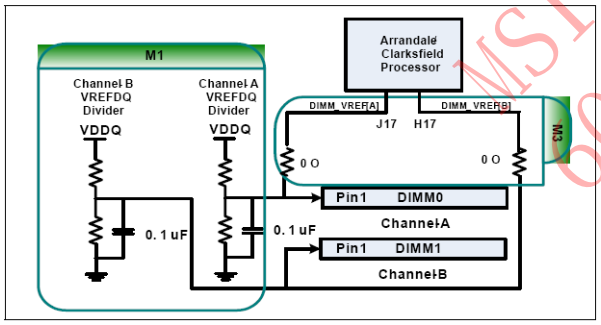


2.5.4 DDR3 VREFDQ Design Implementation

Intel is requesting that customers implement two methods (M1 and M3) to generate and control the DDR3 SO-DIMM Reference voltage for Data/Strobe inputs (V_{REFDQ}) on Arrandale- and Clarksfield-based platforms. For Arrandale, M1 should be used. For Clarksfield only designs and common motherboard designs (which support both Arrandale and Clarksfield processors), both M1 and M3 methods should be con-currently implemented.

Note: DDR3 V_{REFDQ} recommendation outlined above in this document, V_{REFCA} and V_{REFDQ} on SO-DIMM cannot be tied together any more for Clarksfield only and Common motherboard designs in order to support M3 and M1/M3 co-existence.

Figure 33. Clarksfield DDR3 SO-DIMM VREF_DQ Design Requirements



IDD Specification parameters Definition
(IDD values are for full operating range of voltage and Temperature)

Parameter	Symbol	Max	Unit
Operating One bank Active-Precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0	1,200	mA
Operating One bank Active-read-Precharge current; IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD1	1,360	mA
Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P	800	mA
Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q	960	mA
Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD2N	960	mA
Active power - down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD3P	800	mA
Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD3N	1,000	mA
Operating burst read current; All banks open, Continuous burst reads; IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD4R	2,120	mA
Operating burst write current; All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING; IDD4R	IDD4W	2,320	mA
Burst refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD5	2,240	mA
Self refresh current; CK and /CK at 0V; CKE = 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	IDD6	160	mA
Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK =tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are STABLE during Deselects; Data pattern is same as IDD4R	IDD7	3,400	mA

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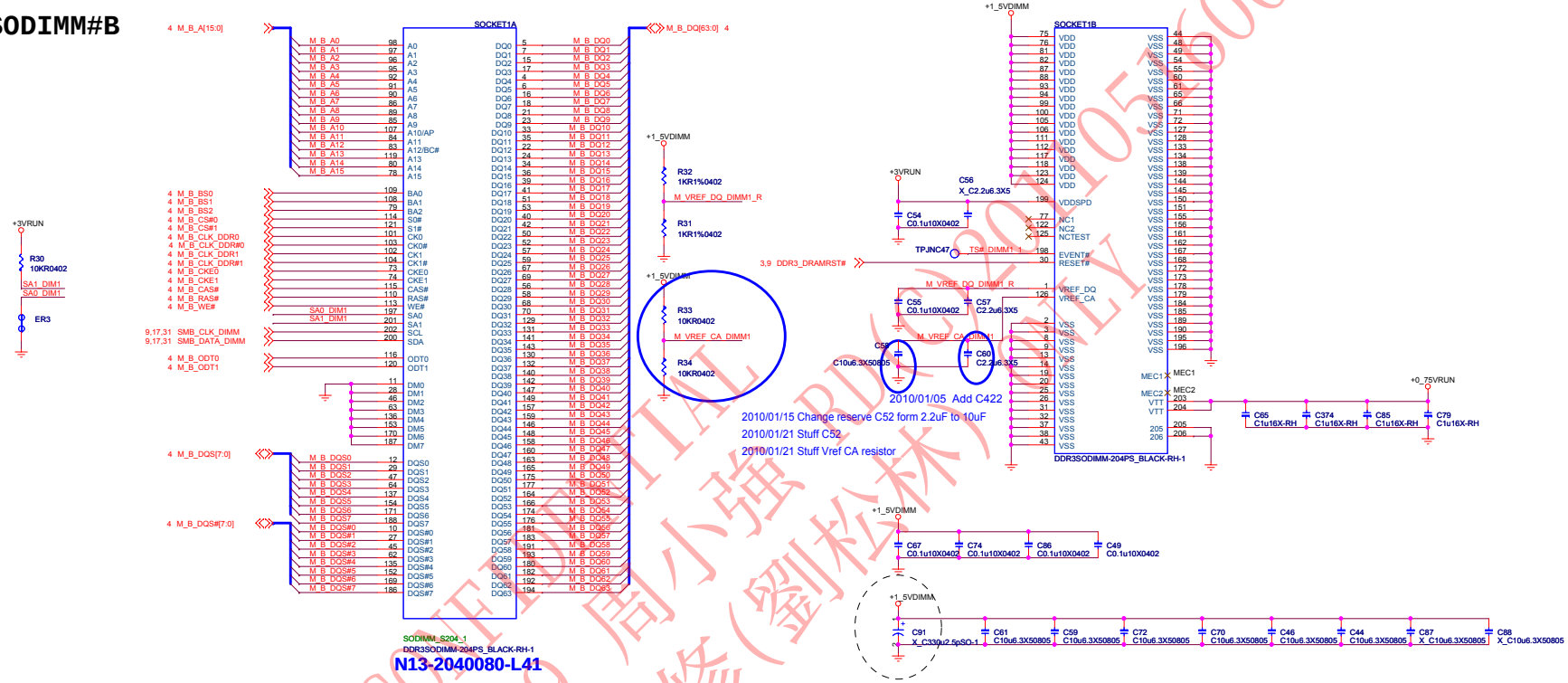
SODIMM#B



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Title: DDR3 SODIMM1

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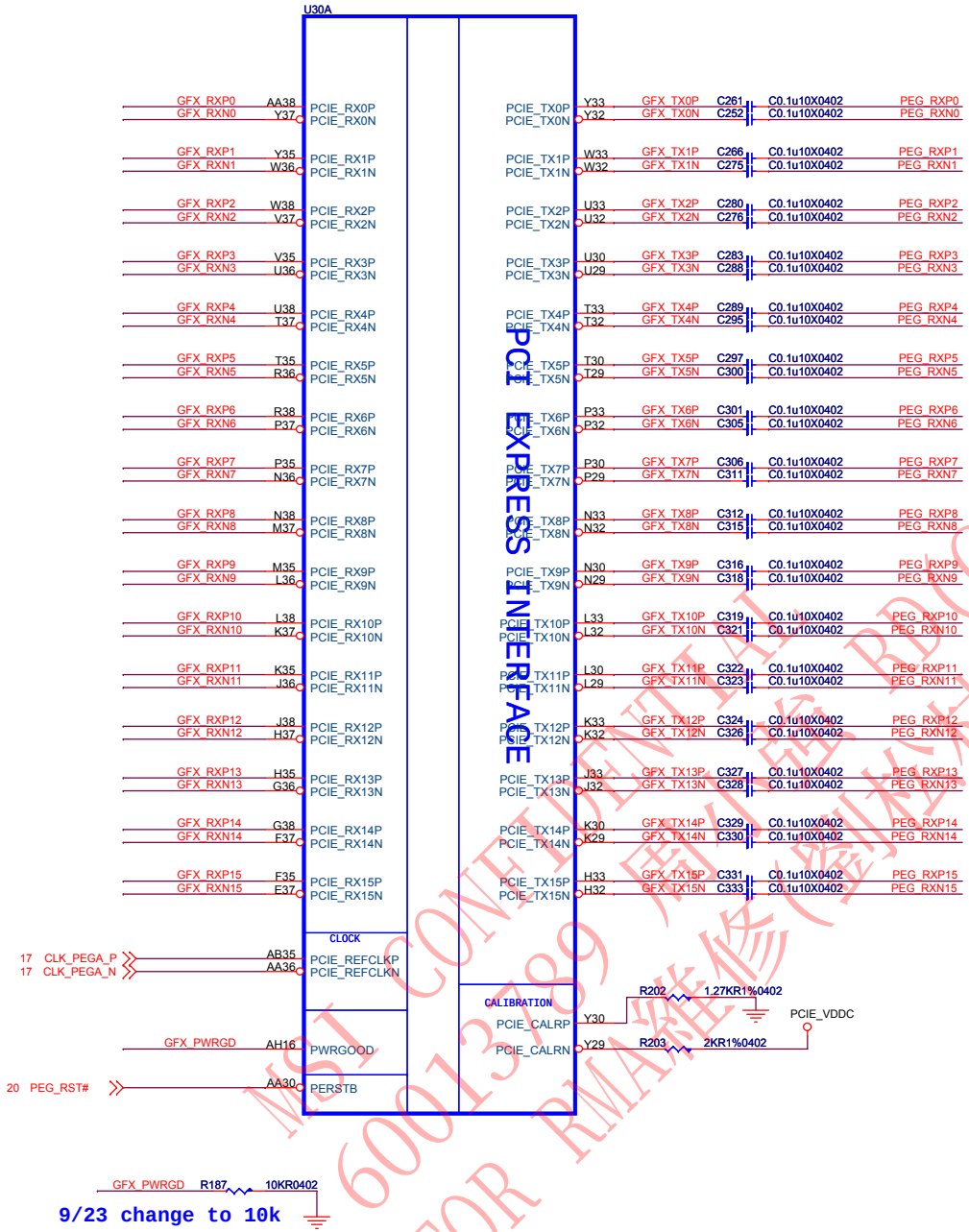

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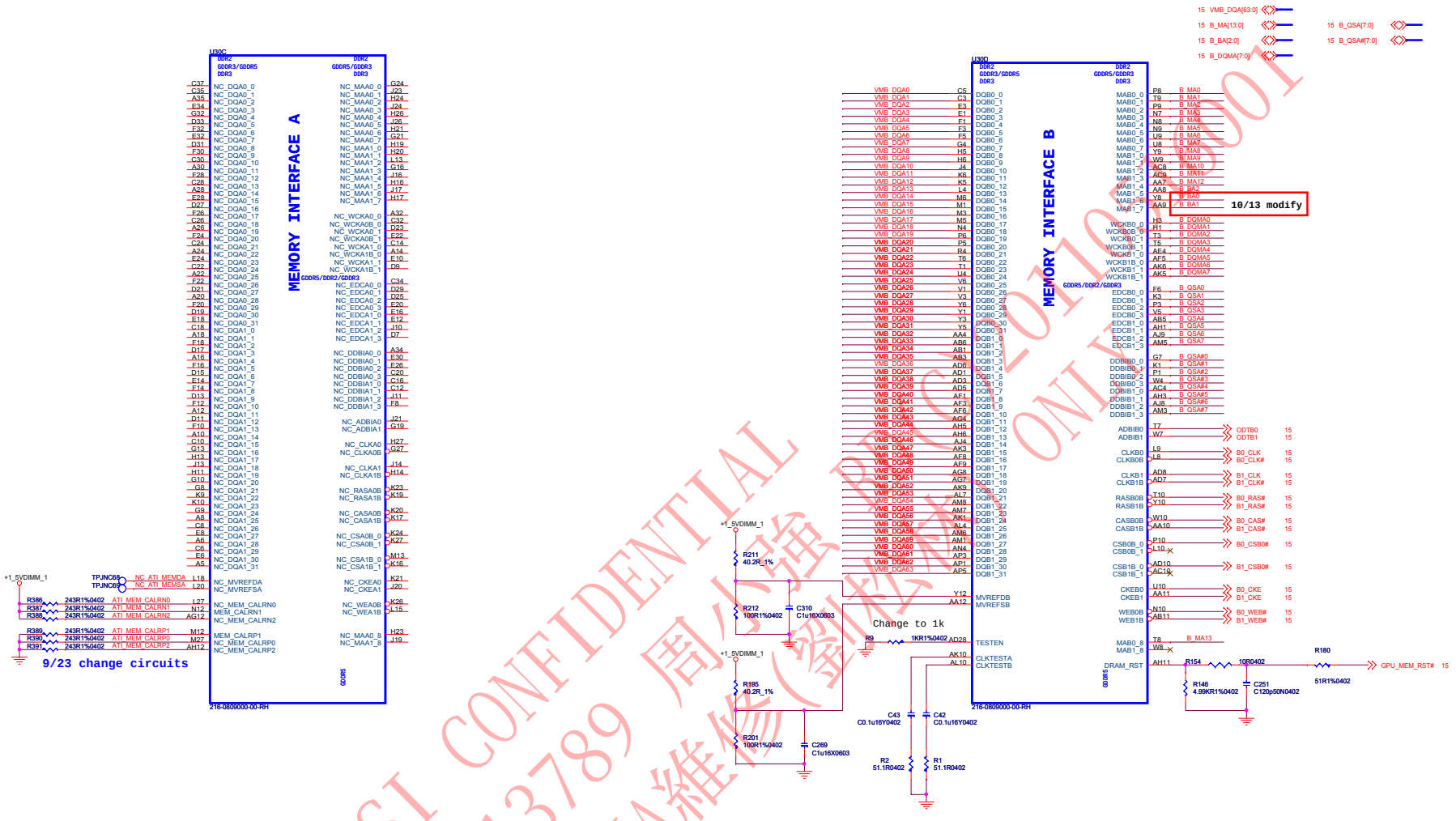

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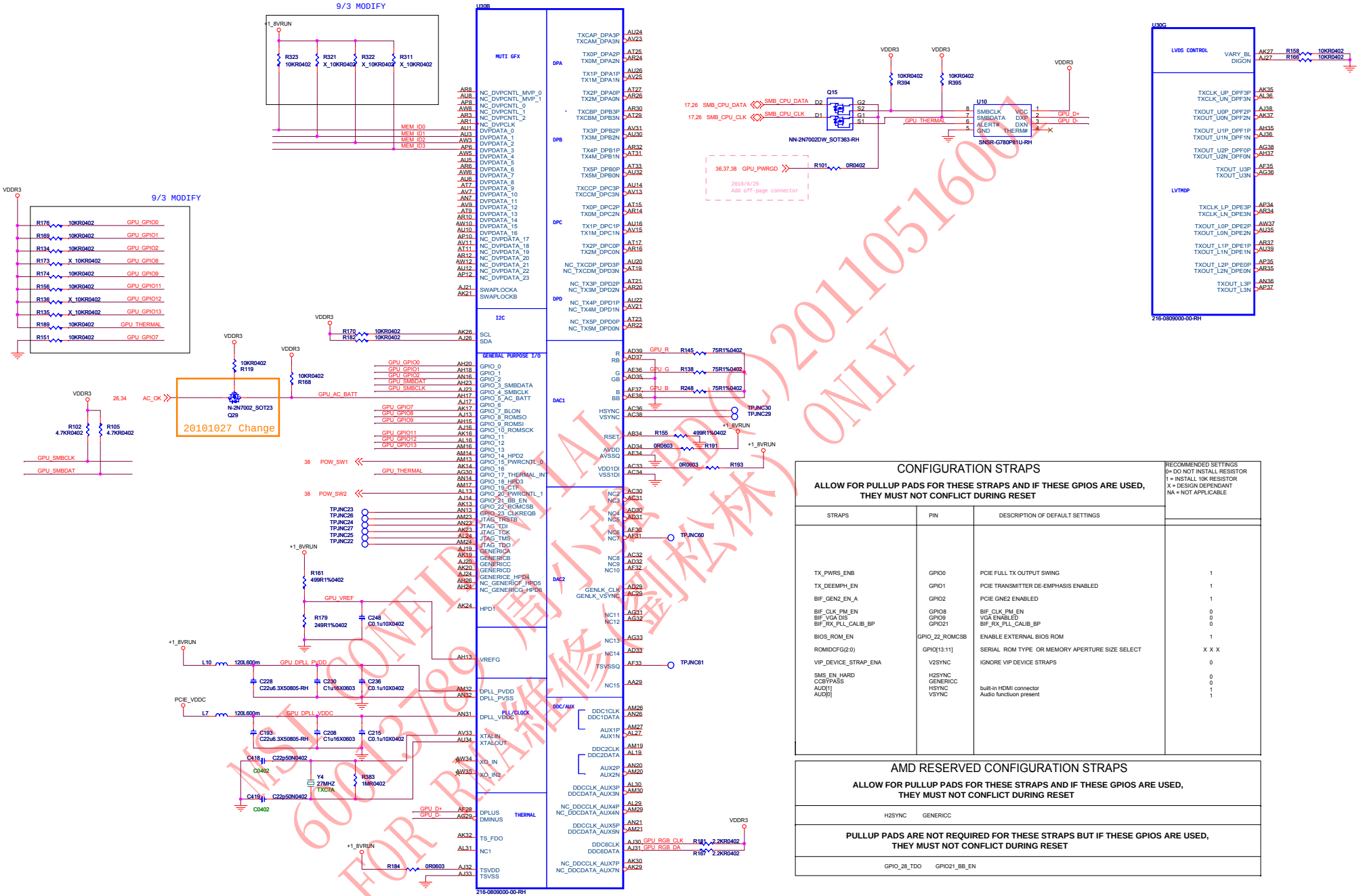

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA'DIS'	GPIO9	VGA ENABLED	0
BIF_RX_PLL_CALIB_BP	GPIO21	BIF_RX_PLL_CALIB_BP	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	1
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
SMS_EN_HARD	H2SYNC		0
CCBYPASS	GENERICC		0
AUD[1]	HSYNC	built-in HDMI connector	1
AUD[0]	VSYNC	Audio functiuon present	1

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO	GPIO21_BB_EN

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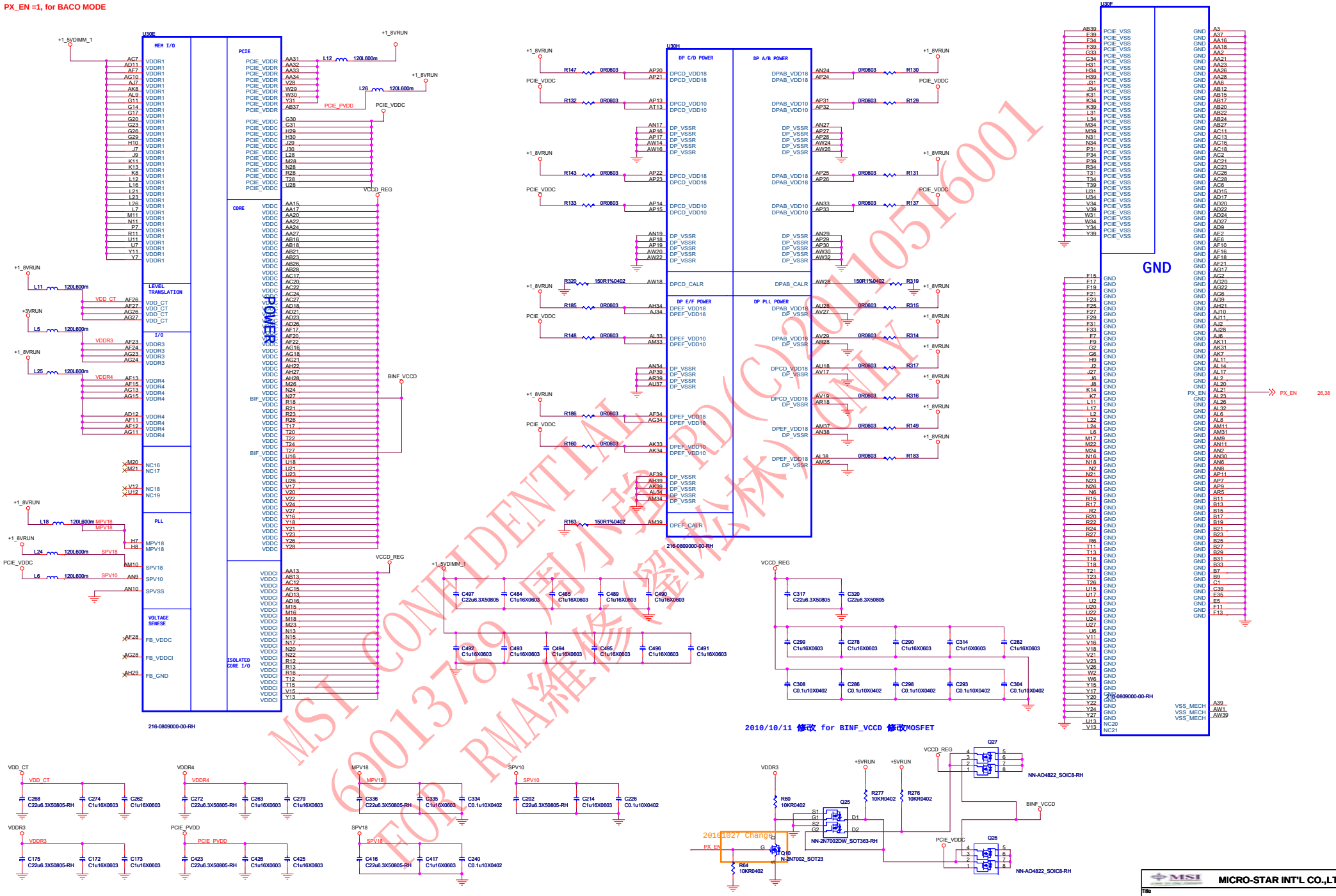
BACO enable just close the core power

PX_EN=0, for Normal Operation

PX_EN =1, for BACO MODE



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Title	ATI VGA PWR GND
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Title	VRAM B		
Size A2	Document Number MS-1482		Rev 0A
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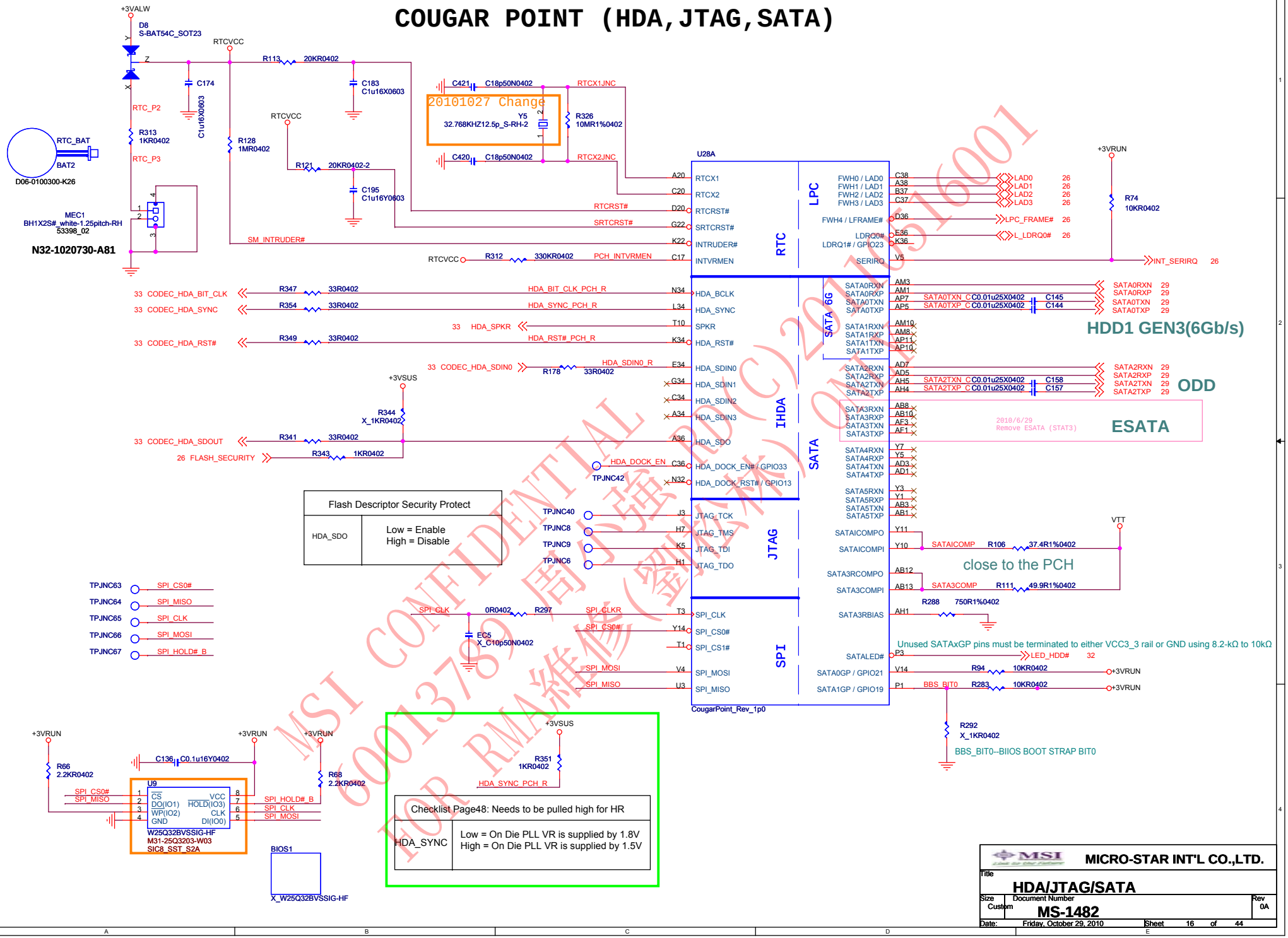
COUGAR POINT (HDA,JTAG,SATA)



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Title: HDA/JTAG/SATA

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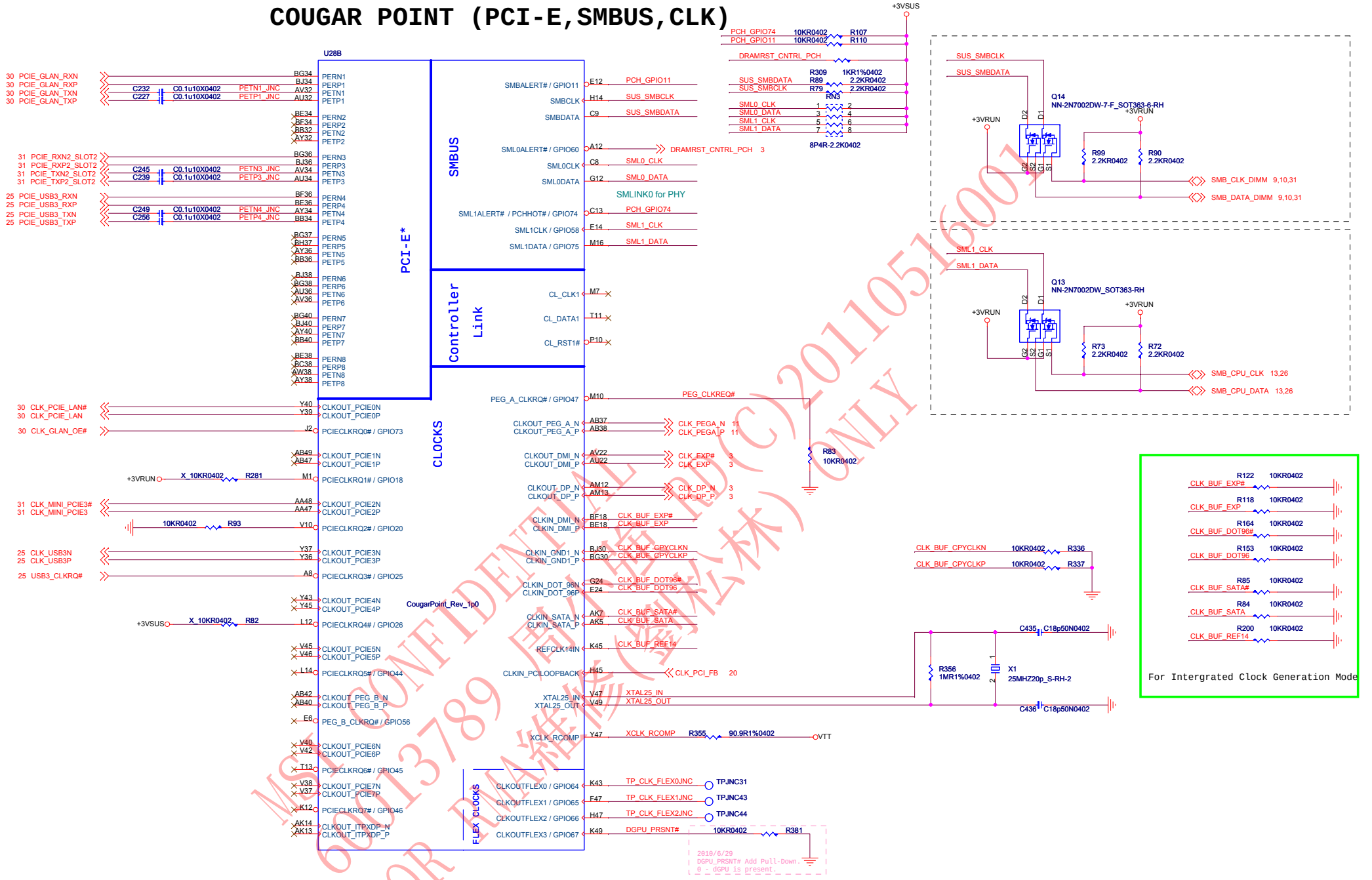
COUGAR POINT (PCI-E,SMBUS,CLK)



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Title	PCI-E/SMBUS/CLK
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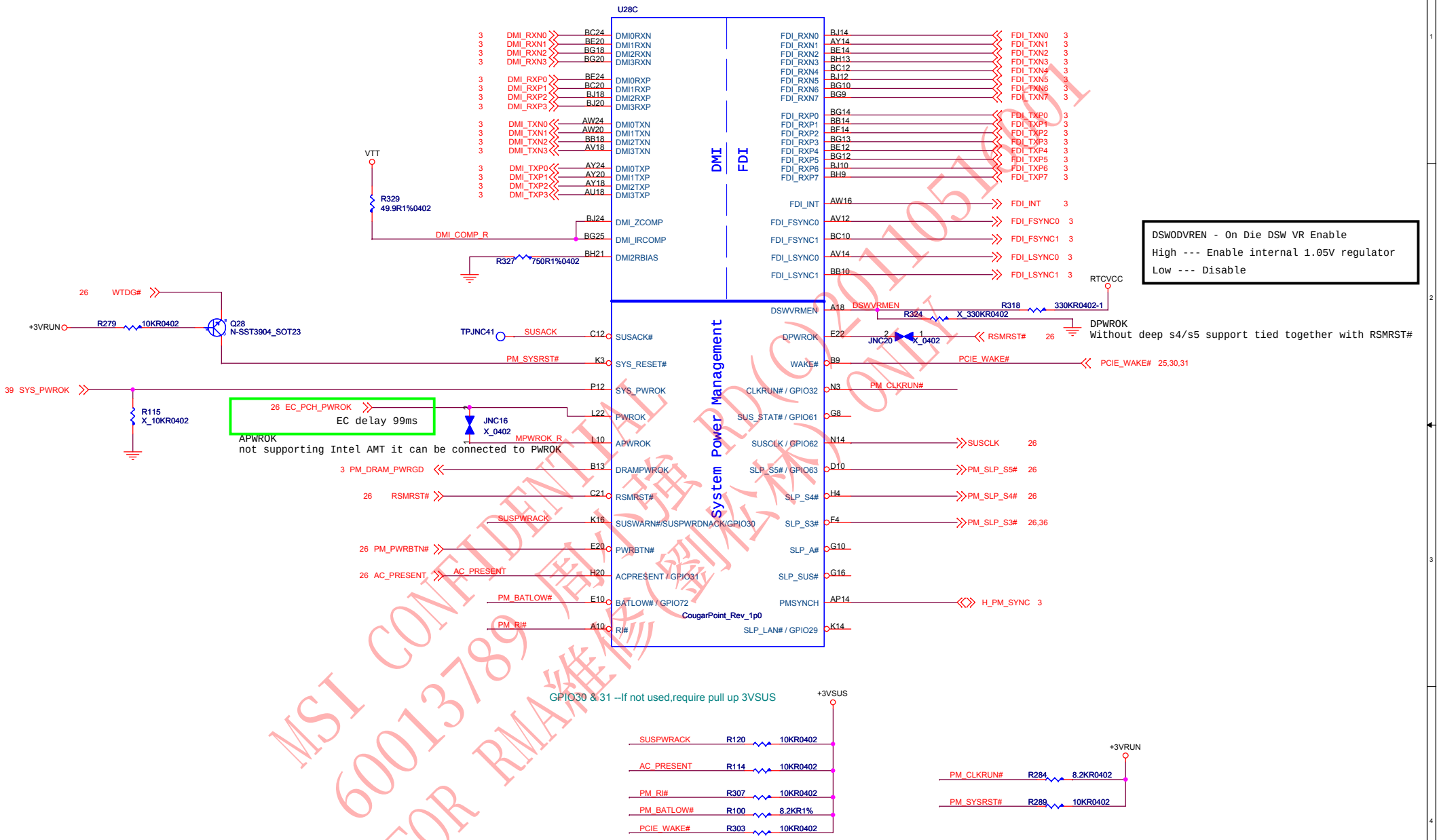
COUGAR POINT (DMI,FDI,GPIO)



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Title: DMI/FDI/GPIO

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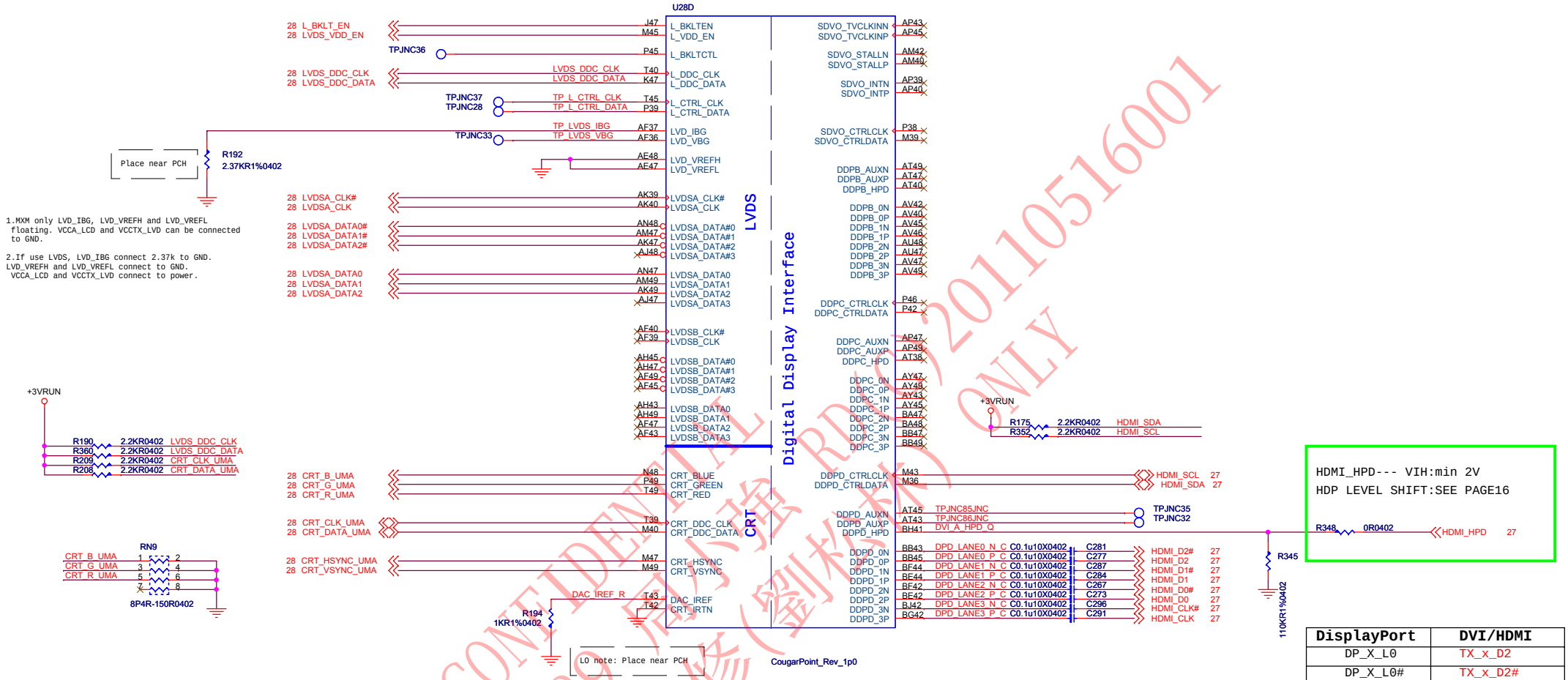
COUGAR POINT (LVDS,DDI)



DisplayPort	DVI/HDMI
DP_X_L0	TX_x_D2
DP_X_L0#	TX_x_D2#
DP_X_L1	TX_x_D1
DP_X_L1#	TX_x_D1#
DP_X_L2	TX_x_D0
DP_X_L2#	TX_x_D0#
DP_X_L3	TX_x_CLK
DP_X_L3#	TX_x_CLK#
DP_X_AUX	DDC_x_CLK
DP_X_AUX#	DDC_x_DATA

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Title: PCH_LVDS/DDI

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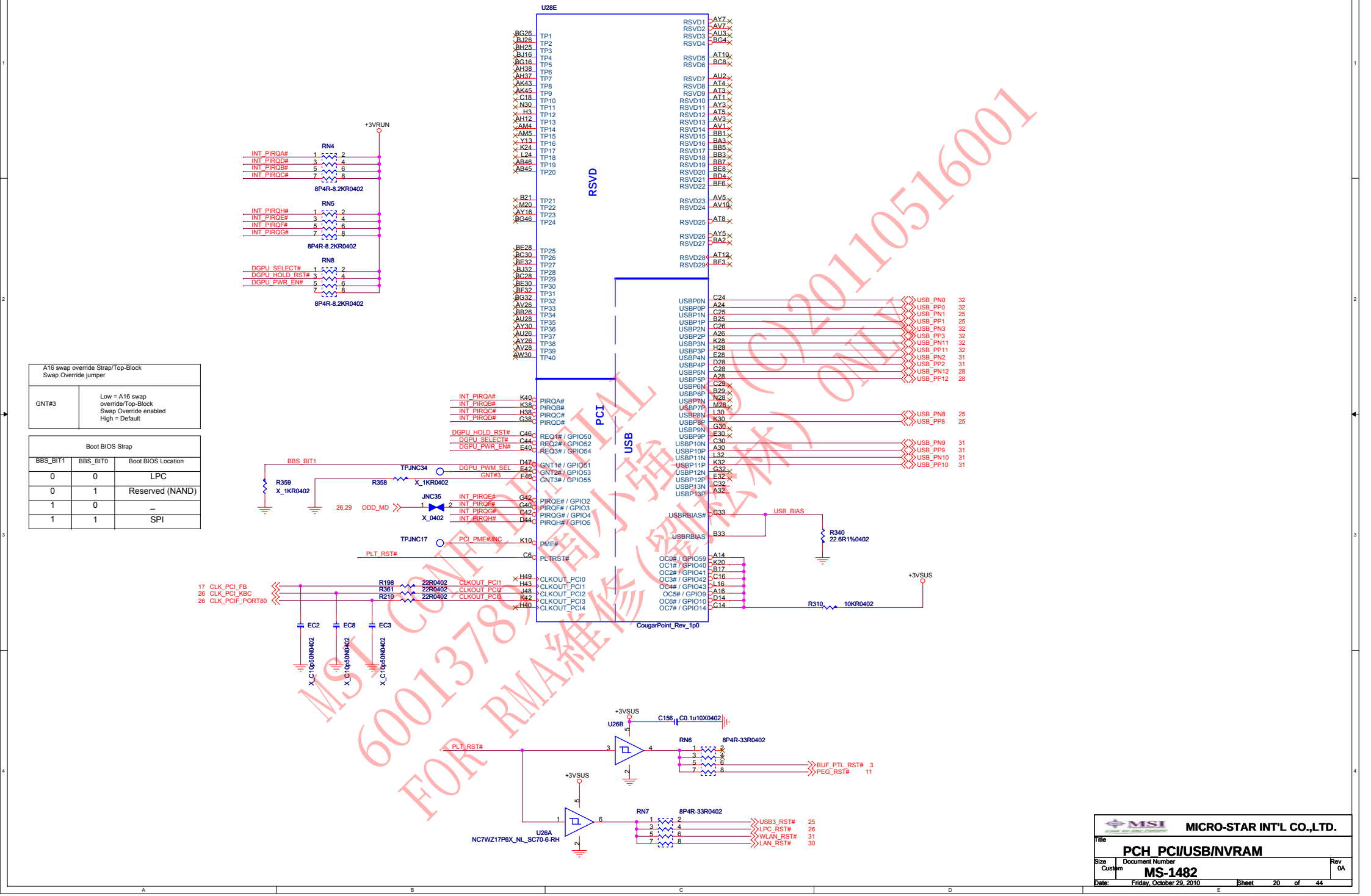
COUGAR POINT (PCI,USB,NVRAM)



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Title	PCH_PCI/USB/NVRAM
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COUGAR POINT (GPIO,VSS_NCTF,RSVD)

GPIO0 & 6 & 16 & 22 & 34 & 38 & 48 --If not used,require pull up 3VRUN
GPIO57 --If not used,require pull up 3VSUS
GPIO15--High is support TLS,internal pull-down
GPIO27 is deep S4 & S5 weak up event,internal pull high.& It's VCCFDIPLL internal VRM strapping pin
GPIO35 --Define to EDID Select (If not used,require pull down)

Integrated Clock Chip Enable	
ICC_EN	High: use CK505 (buffer through mode) intelnal pull high
	Low: use PCH(interated clock mode)

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable

DMI termination voltage override	
GPIO36	Low-- TX,RX terminated to same vlotage (DC coupling mode)default

GPIO36 --CRB connector to 3V

FDI termination voltage override	
GPIO37	Low-- TX,RX terminated to same vlotage (DC coupling mode)default

U28F

GPIO
BMBUSY# / GPIO0 T7
TACH1 / GPIO1 A42
TACH2 / GPIO6 H36
TACH3 / GPIO7 E38
GPIO8 C10
LAN_PHY_PWR_CTRL / GPIO12 C4
GPIO15 G2
SATA4GP / GPIO16 U2
TACH0 / GPIO17 D40
SCLOCK / GPIO22 T5
GPIO24 / MEM_LED E8
GPIO27 E16
GPIO28 P8
STP_PCI# / GPIO34 K1
GPIO35 K4
SATA2GP / GPIO36 V8
SATA3GP / GPIO37 M5
SLOAD / GPIO38 N2
SDATAOUT0 / GPIO39 M3
SDATAOUT1 / GPIO48 V13
SATA5GP / GPIO49 V3
GPIO57 D6

CPU/MISC
TACH4 / GPIO68 C40
TACH5 / GPIO69 B41
TACH6 / GPIO70 C41
TACH7 / GPIO71 A40
A20GATE P4
PECI AU16
RCIN# P5
PROCPWRGD AY11
THRMTRIP# AY10
INIT3_3V# T14
DF_TVS AY1
TS_VSS1 AH8
TS_VSS2 AK11
TS_VSS3 AH10
TS_VSS4 AK10
NC_1 P37

NCTF
VSS_NCTF_1 A4
VSS_NCTF_2 A44
VSS_NCTF_3 A45
VSS_NCTF_4 A46
VSS_NCTF_5 A5
VSS_NCTF_6 A6
VSS_NCTF_7 B3
VSS_NCTF_8 B47
VSS_NCTF_9 BD1
VSS_NCTF_10 BD49
VSS_NCTF_11 BE1
VSS_NCTF_12 BE49
VSS_NCTF_13 BF1
VSS_NCTF_14 BF49
VSS_NCTF_15 BG2
VSS_NCTF_16 BG48
VSS_NCTF_17 BH3
VSS_NCTF_18 BH47
VSS_NCTF_19 BJ4
VSS_NCTF_20 BJ44
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VSS_NCTF_23 BJ5
VSS_NCTF_24 BJ6
VSS_NCTF_25 C2
VSS_NCTF_26 C48
VSS_NCTF_27 D1
VSS_NCTF_28 D49
VSS_NCTF_29 E1
VSS_NCTF_30 E49
VSS_NCTF_31 F1
VSS_NCTF_32 F49

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+3VRUN
R385 10KR0402
ODD_PWR_EN 29
R75 10KR0402 GPIO0
26 KBSMI#
R188 10KR0402 DGPU_HPD_INTR#
26 KBSCI#
+3VSUS
R308 1KR0402 ICC_EN#
TPJNC7
R294 X_1KR0402 HOST_ALERT#1
R291 10KR0402 JTAG_SATA4GP
DGPU_PWROK
R80 10KR0402 BIOS_REC
+3VSUS
R295 10KR0402 HOST_ALERT#2
R117 X_1KR0402 DSW weak up event
R92 X_1KR0402 PLL_ODVR_EN
R290 10KR0402 STP_PCI#
2010/6/29 EDID_SELECT# add test Point
TPJNC51 EDID_SELECT#
R76 200KR0402 GPIO36
29 ODD_DP
GPIO37
R293 10KR0402 MFG_MODE
CRB_SV_DET
R95 10KR0402 TEST_SET_UP
TPJNC39 CRIT_TEMP_REP#
+3VSUS R97 10KR0402 GPIO57
+3VRUN R81 X_1KR0402
PR46 100KR0402
DGPU_PWROK R350 10KR0402
H_A20GATE 26
R301 X_0R0402 H_PECI 3,26
KBRST# 26
H_CPUPWRGD 3
PCH_THRMTRIP# R R300 390R0402_1% H_THRMTRIP# 3
Thrmtrip不用pull 1.05V
+1_8VRUN
R298 2.2KR0402
NV_CLE R299 1KR0402 H_SNB_IVB# 3
Change to 1K
R109 0R0402
R77 0R0402
R104 0R0402
R78 0R0402

Intel Comments:
Reserve 0 ohm option in these pins
pins AH8, AK11, AH10 & AK10) to GND.

DMI & FDI Termination Voltage	
NV_CLE	Set to VSS when LOW
	Set to VCC when High

+3VRUN
CRB_SV_DET R282 X_10KR0402
R296 100KR0402

CRB_SV_DET	
GPIO39	High: External GFX
	Low: Internal GFX

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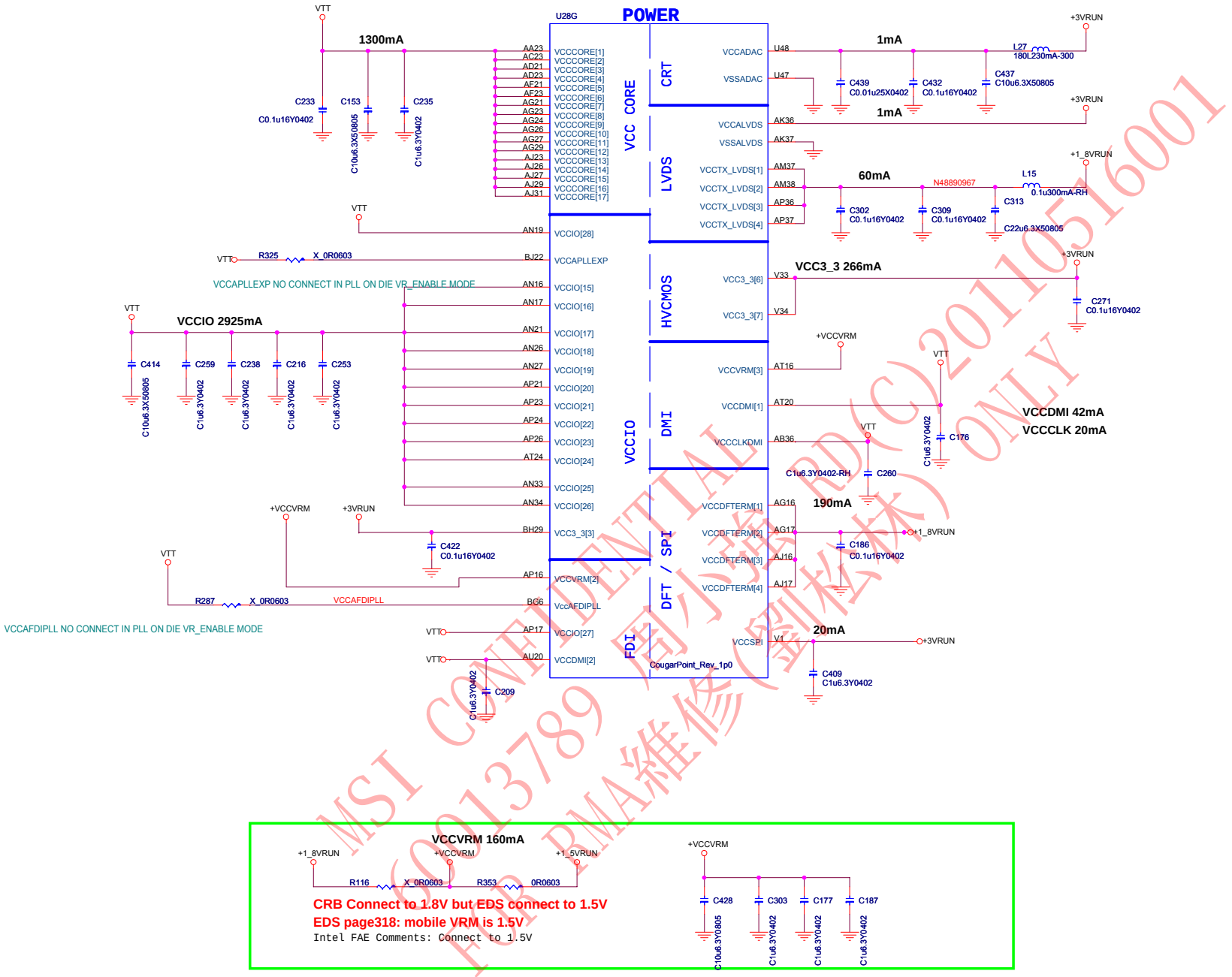
MICRO-STAR INT'L CO.,LTD.
Title: PCH_GPIO/NCTF/RSVD
Size: Custom | Document Number: MS-1482 | Rev: 0A
Date: Friday, October 29, 2010 | Sheet 21 of 44

COUGAR POINT (POWER)



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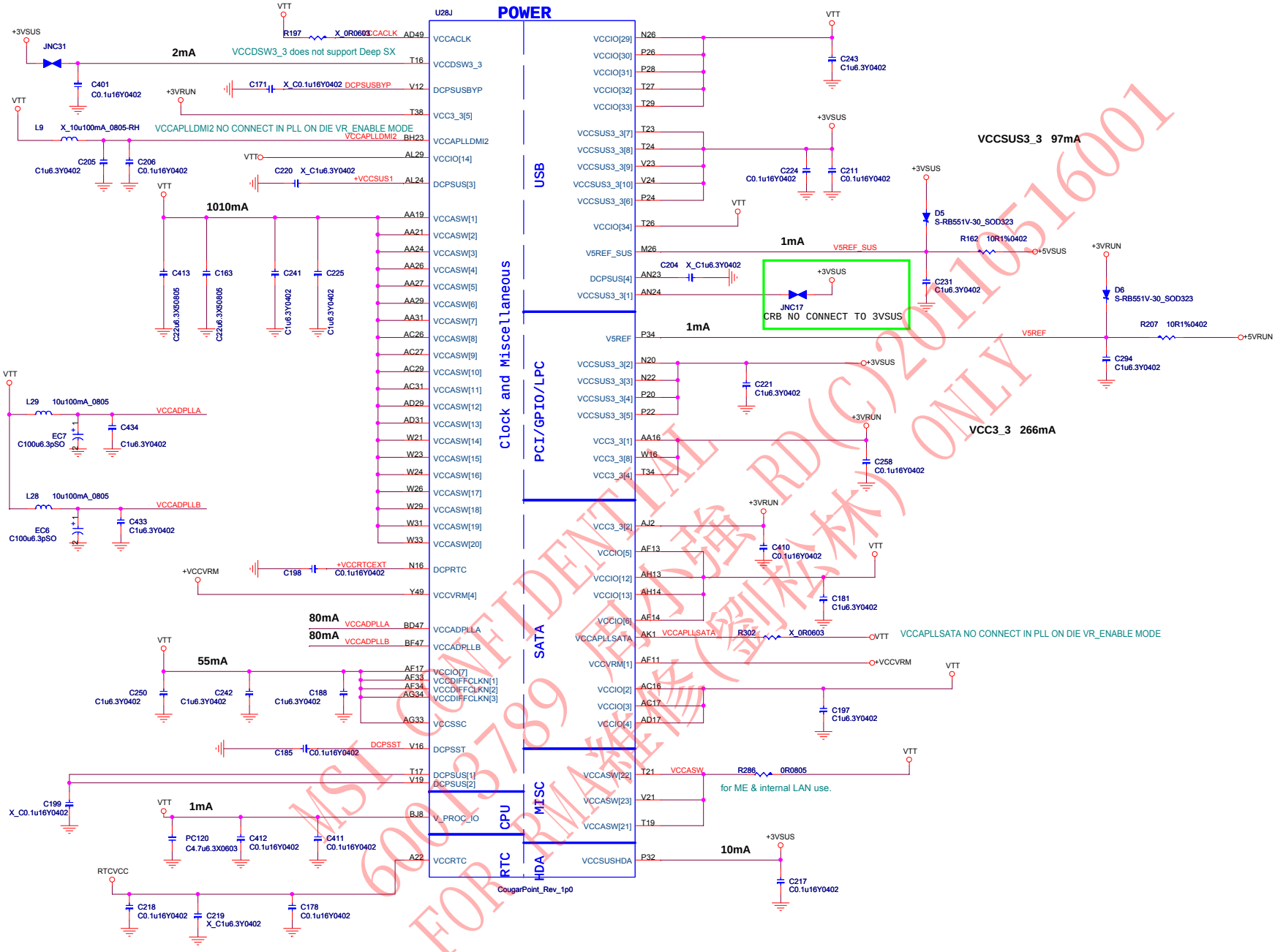
FOR RMA維修(劉松林) ONLY

VCCVRM 160mA

CRB Connect to 1.8V but EDS connect to 1.5V
EDS page318: mobile VRM is 1.5V
Intel FAE Comments: Connect to 1.5V

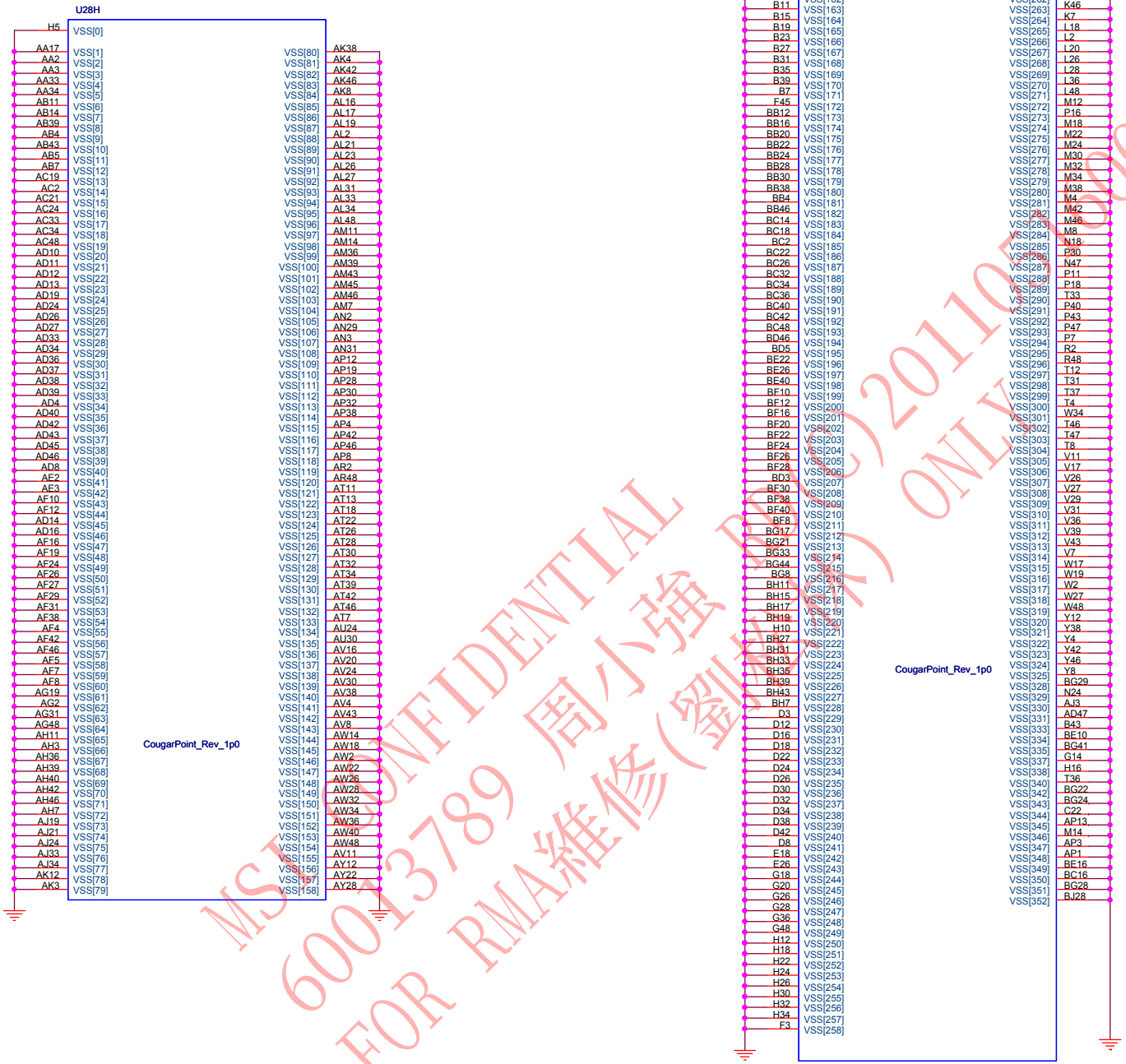
MSI	MICRO-STAR INT'L CO.,LTD.
Title	PCH_POWER
Size: Custom	Document Number: MS-1482
Rev	0A
Date: Friday, October 29, 2010	Sheet 22 of 44

COUGAR POINT (POWER)



MICRO-STAR INT'L CO.,LTD.			
Title: PCH_POWER2			
Size: Custom	Document Number: MS-1482		Rev: 0A
Date: Friday, October 29, 2010	Sheet 23 of 44		

Cougar Point (GND)



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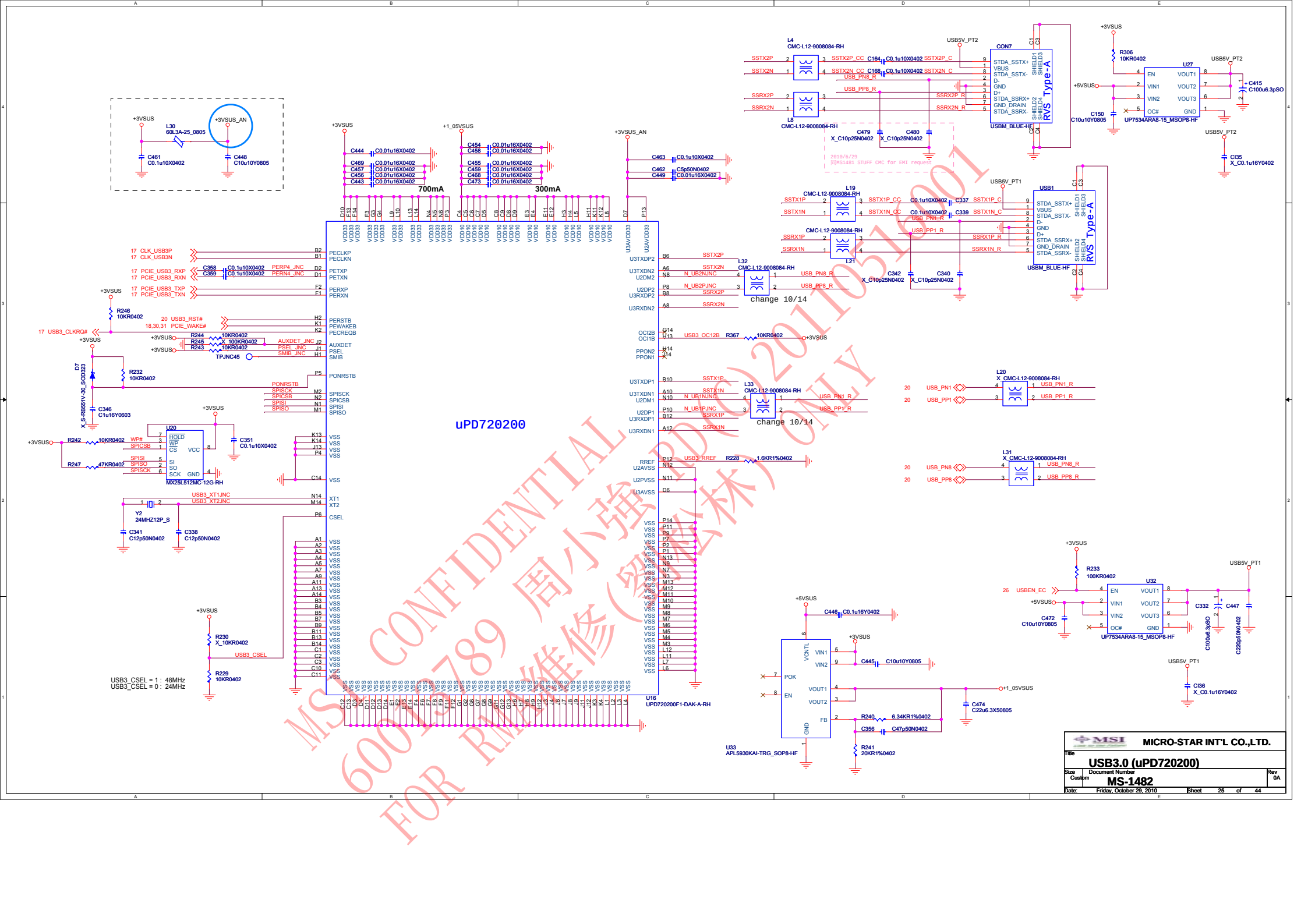
MICRO-STAR INT'L CO.,LTD.

Title: PCH_GND

Size: Custom | Document Number: MS-1482 | Rev: 0A

Date: Friday, October 29, 2010 | Sheet 24 of 44


uPD720200
U16
UPD720200F1-DAK-A-RH
700mA
300mA
change 10/14
change 10/14
MX25L512MC-12G-RH
UP7534ARA8-15_MSOP8-HF
APL5930KAI-TRG_SOP8-HF
USBM_BLUE-HF
RVS Type-A
USB3_CSEL = 1 : 48MHz
USB3_CSEL = 0 : 24MHz
MICRO-STAR INT'L CO.,LTD.
USB3.0 (uPD720200)
MS-1482
Friday, October 29, 2010
Sheet 25 of 44
CONFIDENTIAL
FOR R&D ONLY

10/20修改料號為 B02-0393014-E18

Change to High Active

2010/6/29 MS1481 機構 只能支援POWER LED & P1 LED(Turbo)

20101007 Change

USE SUSCLK:R35、 R141 Stuff ; Y5、C107、C106 No Stuff
USE Crystal:R35、 R141 No Stuff ; Y5、C107、C106 Stuff

NEW FUNCTION

EMI REQUEST

N5A-14F0110-A81

N5A-25F0110-A81

N32-1140060-H06

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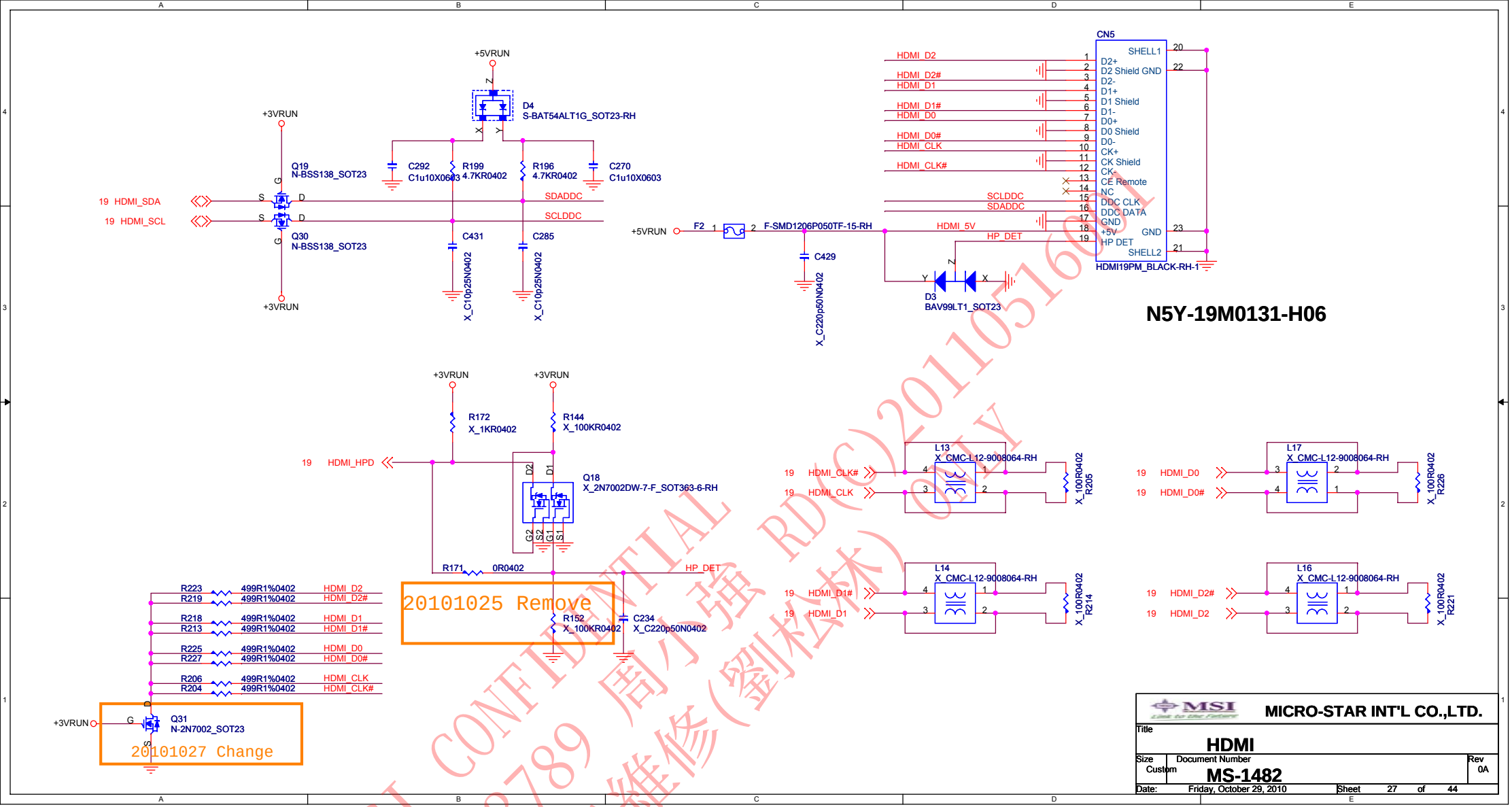
Title	KBC 3930
Size / Document Number	Custom / MS-1482
Rev	0A
Date	Friday, October 29, 2010
Sheet	26 of 44

MICRO-STAR INT'L CO.,LTD.



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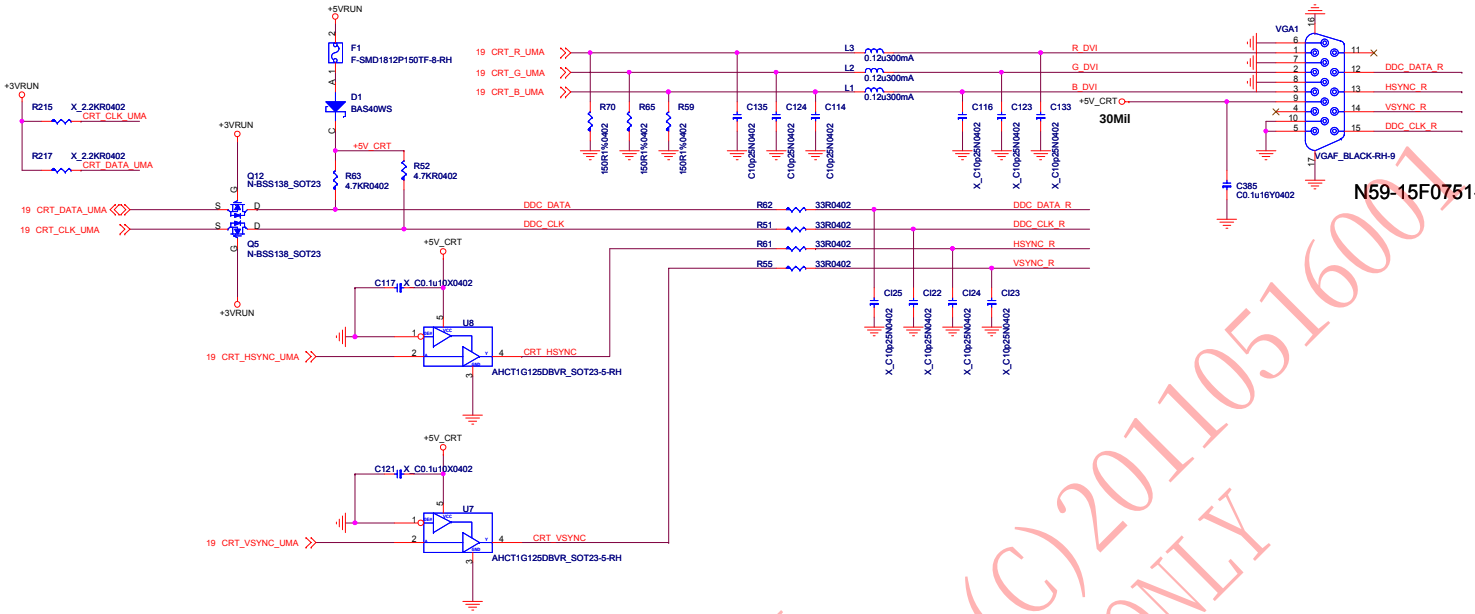
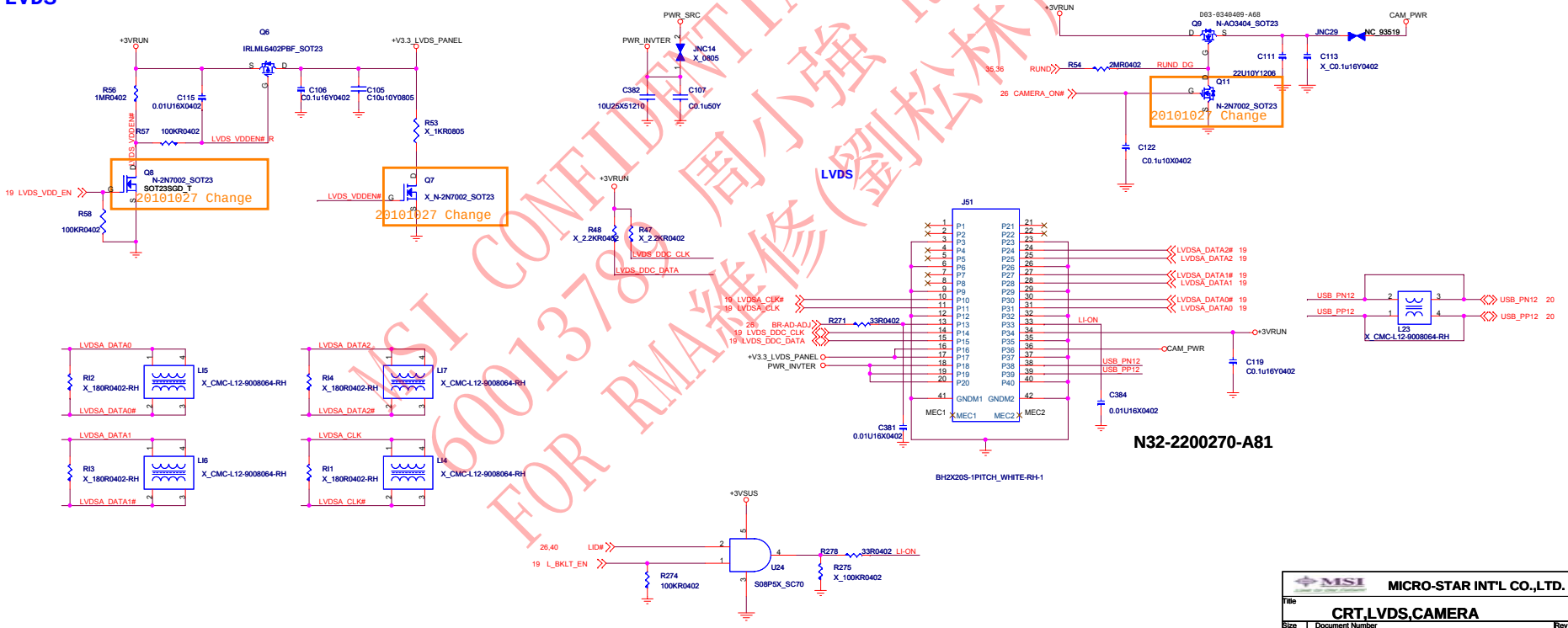
FOR RMA維修(劉松林) ONLY

CRT



N59-15F0751-A10

LVDS



N32-2200270-A81

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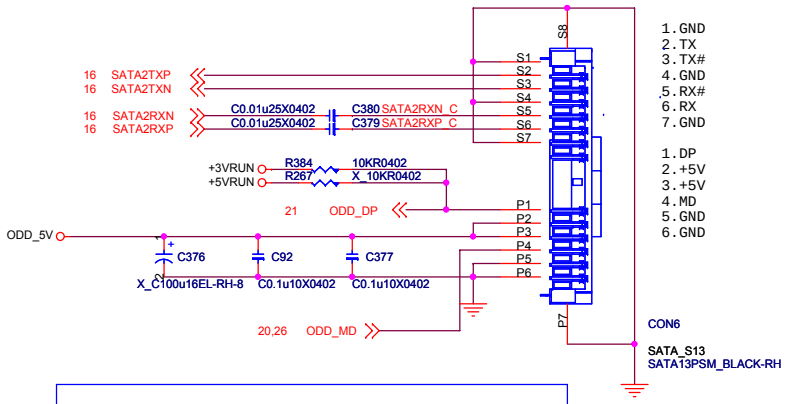
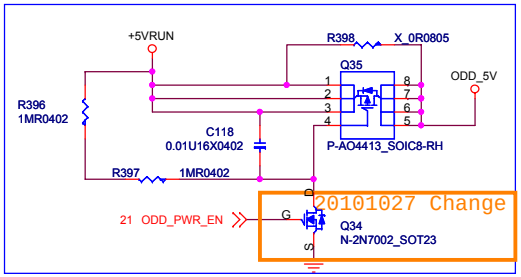
FOR RMA维修(劉松林) ONLY

MICRO-STAR INT'L CO.,LTD.	
Title	CRT,LVDS,CAMERA
Size: Custom	Document Number: MS-1482
Rev: 0A	
Date:	Sheet 28 of 44

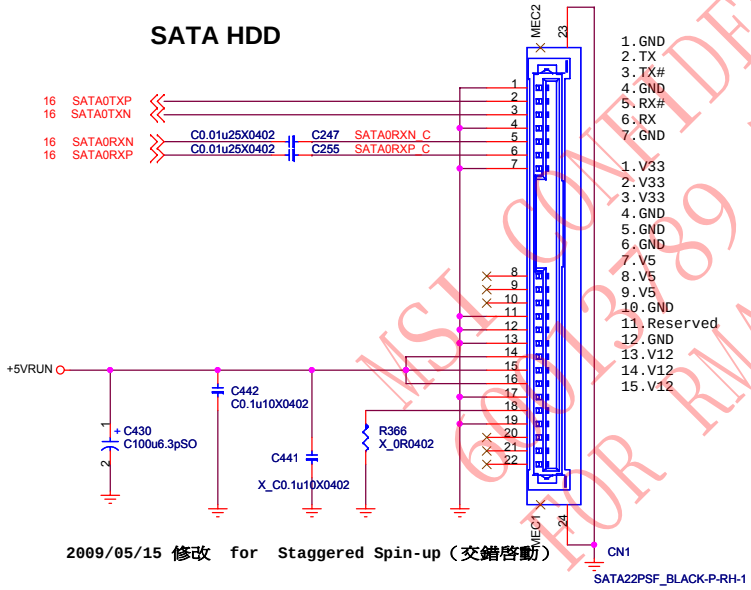
SATA ODD





N5N-13M0010-A81

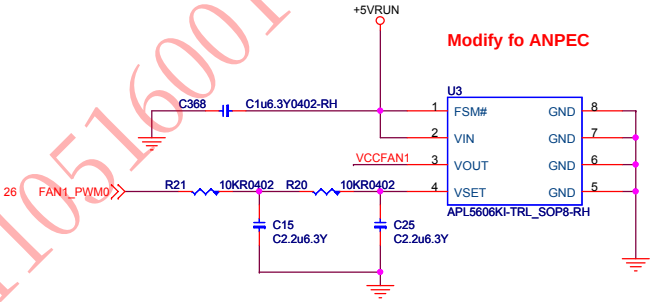
SATA HDD

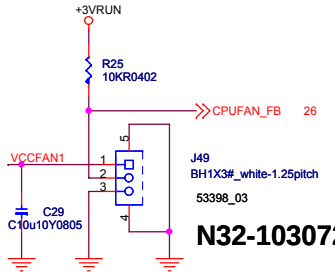


2009/05/15 修改 for Staggered Spin-up（交錯啓動）

N5N-22F0160-A81

CPU FAN





9/10 chage footprint

N32-1030720-A81

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MICRO-STAR INT'L CO.,LTD.

Title: ODD,HDD,FAN

Size: A3 | Document Number: MS-1482 | Rev: 0A

Date: | Sheet 29 of 44

Note: add 0.1u cap at each power pin of LAN, please don't save.

Use External 1.05V Supply When Disable Switch Regulator.
If Using External 1.2V Supply Pls. Contact With FAE.

2010/01/08 remove it,If used jump write

2010/03/03 modify CHOKE1 form 2.2uH to 4.7uH for Realtek request

For RTL8105E
* C1841 to C1844 are for VDD10 pins-- 3, 13, 29, 45.

For RTL8111E
* C1841 to C1848 are for VDD10 pins-- 3, 6, 9, 13, 29, 41, 45.

Part Reference	Choke1	C1840	C1846	R1662	R1668
Enable Switch Regulator					
Disable Switch Regulator	X	X	X	X	X

2010/04/14 modify R21 from 0R to xcopper for cost down

Pls. refer to 8111E Layout Guide for L1, C1, C2 selection criteria.

Remove For Disable Switch Regulator (Accept External 1.05V Power Supply)

For RTL8105E
* C1851 to C1855 are for VDD33 pins-- 27, 39, 42, 47, 48.

For RTL8111E
* C1851 to C1856 are for VDD33 pins-- 12, 27, 39, 42, 47, 48.

VDD33 power on rise time >1ms

C1851 to C1856 Close To LAN chip

2010/04/14 modify R18 from 0R to xcopper for cost down

Remove For Disable Switch Regulator

Please close to LAN Chip

2010/01/04 follow reference schematic add 10K pull low

2010/04/12 modify R16 from 0R to xcopper for cost down

N55-08F0491-SH4

EEPROM Select

For RTL 8105E

VDD33

R11 1K GPO

2.When using EFuse/BIOS Patch.

FOR RTL 8111E

VDD33

R11 1K GPO

R19 10K SMBDATA

3.When using EFuse/BIOS Patch without ASF function.

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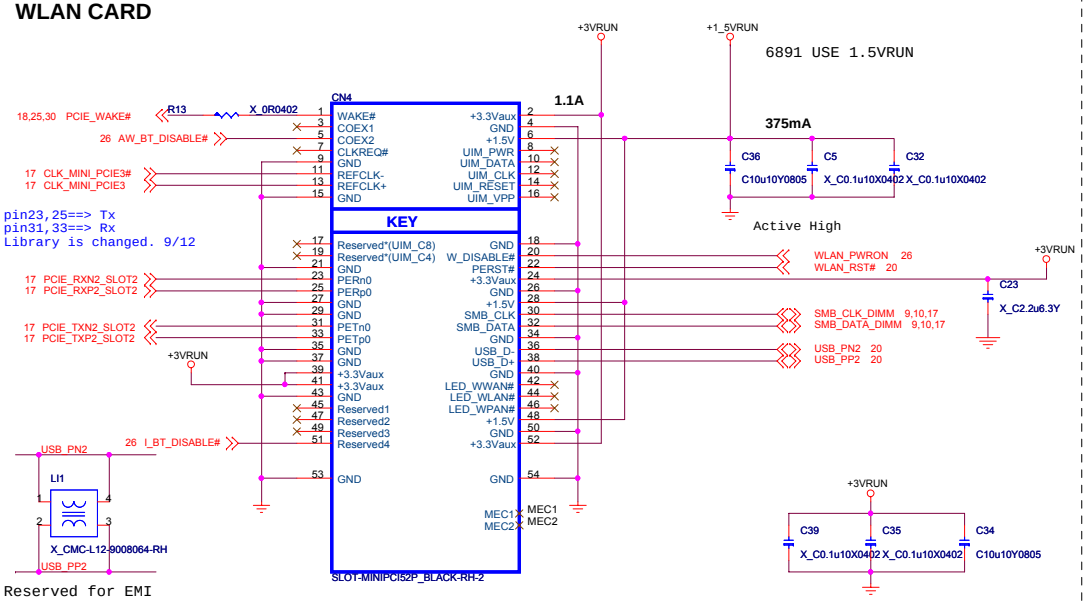
Title: GIGA LAN(RTL 8111EL)

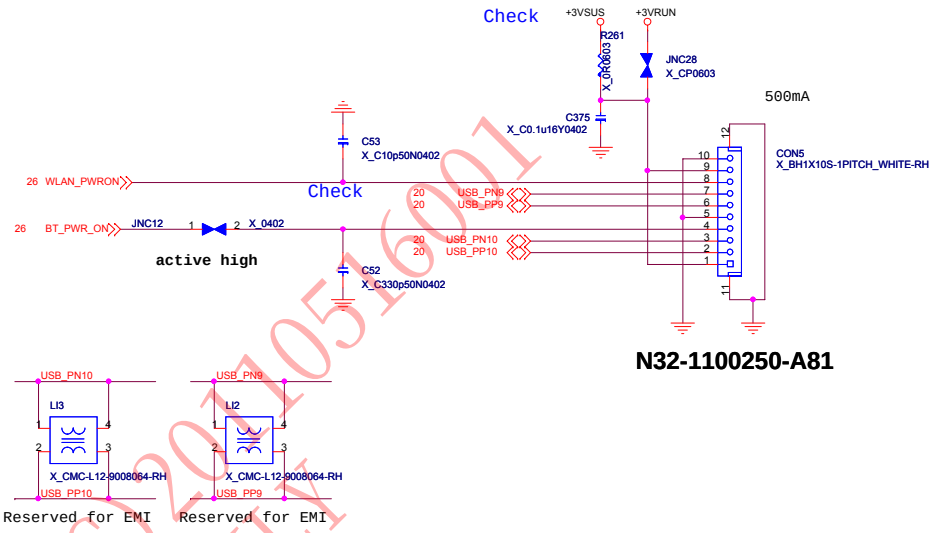
Size: Custom | Document Number: MS-1482 | Rev: 0A

Date: | Sheet 30 of 44

WLAN CARD



MS-3871 BT & WLAN COMBO



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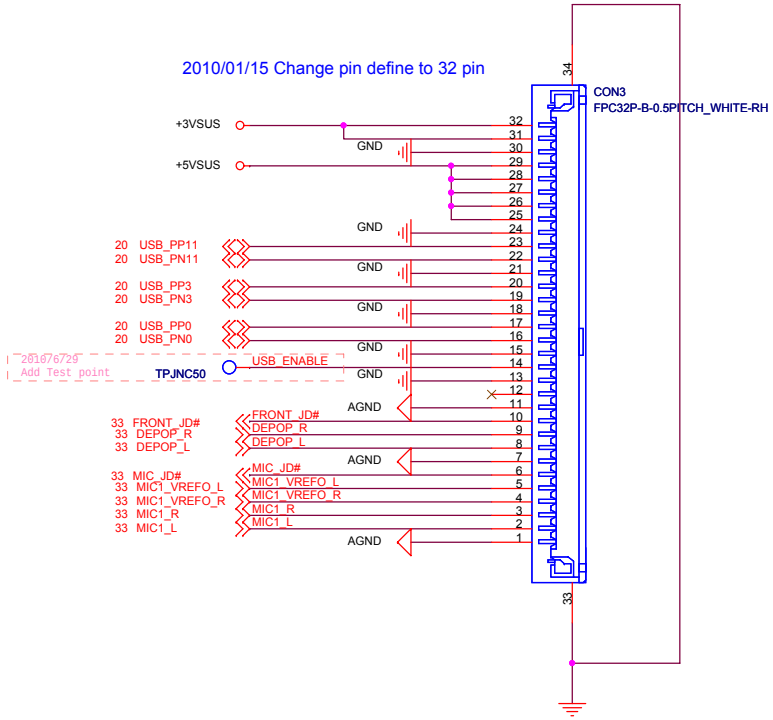
MICRO-STAR INT'L CO.,LTD.

Title: WLAN,BT,Combo

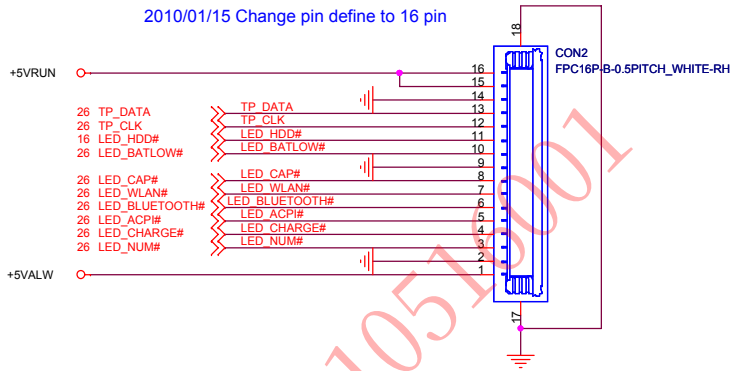
Size: Custom | Document Number: MS-1482 | Rev: 0A

Date: Friday, October 29, 2010 | Sheet 31 of 44



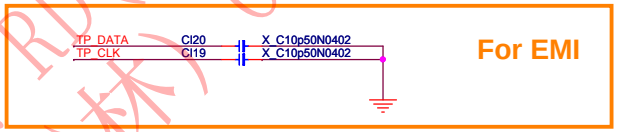
N5A-32F0030-A81

Connector to P.44 Board A

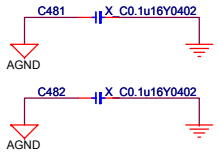


N5A-16F0110-A81

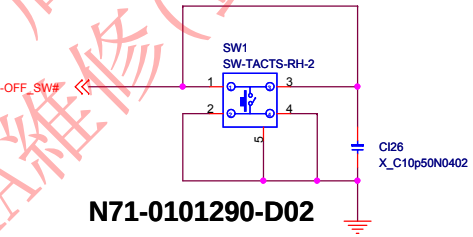
Connector to P.46 Board C



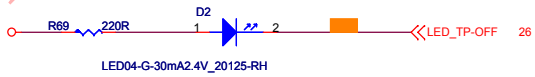
2010/6/29
EMI REQUEST
Bottom Side
X:Y location
(4290.00 -6062.50)
(5035.00 -5815.00)



TP-OFF SW &LED



N71-0101290-D02



D0C-0400500-L05

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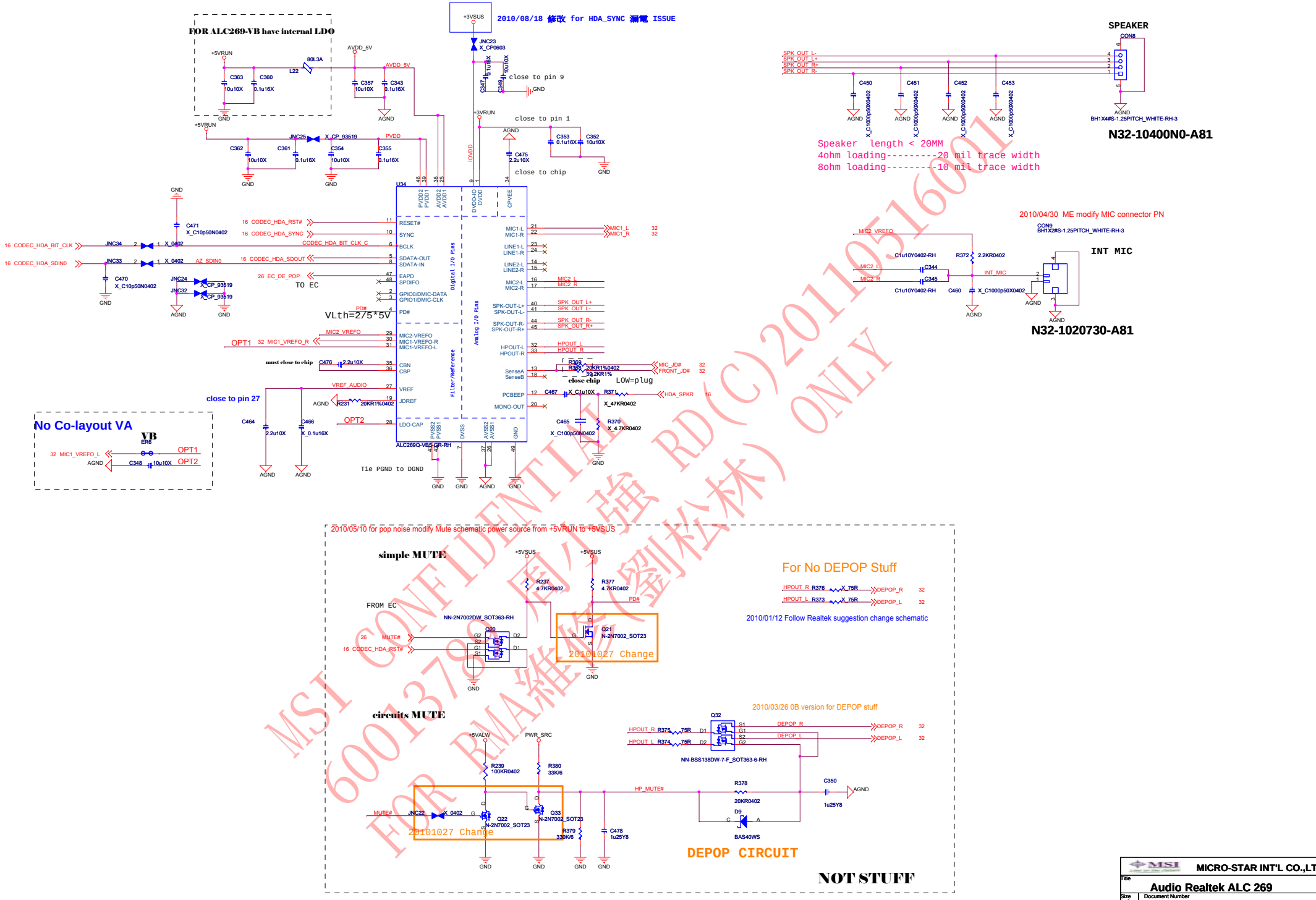
MICRO-STAR INT'L CO.,LTD.

Title: MDC,USB,CONN

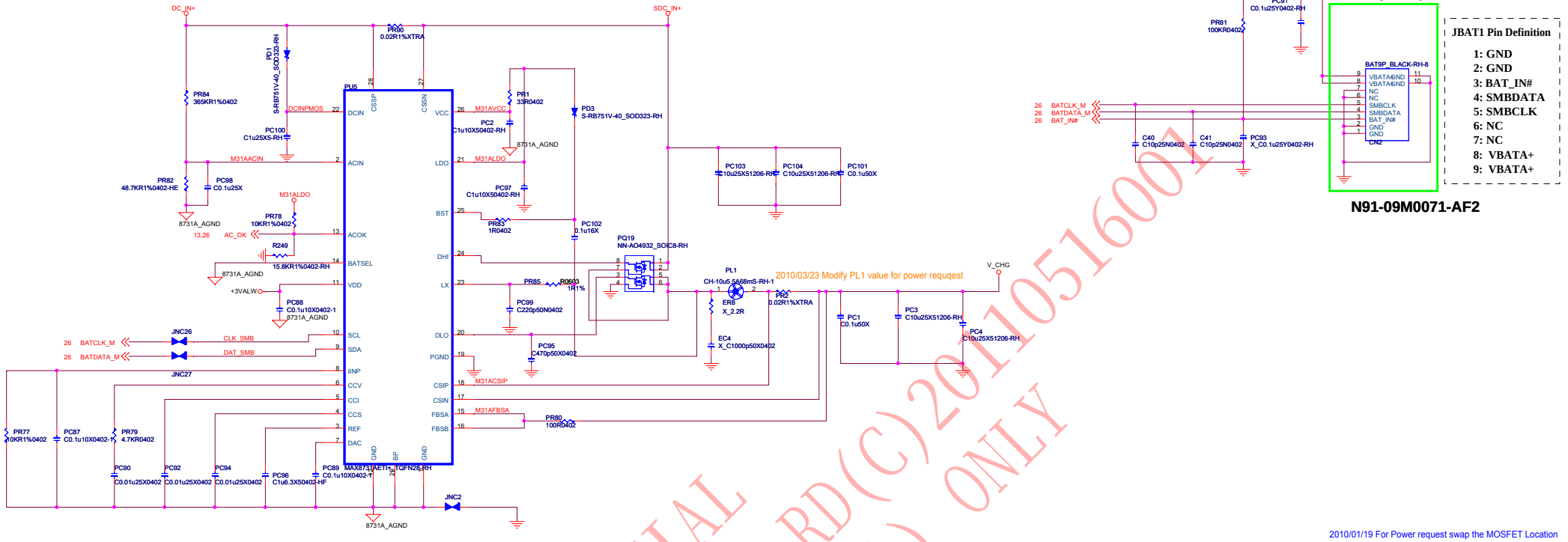
Size: A3 | Document Number: MS-1482 | Rev: 0A

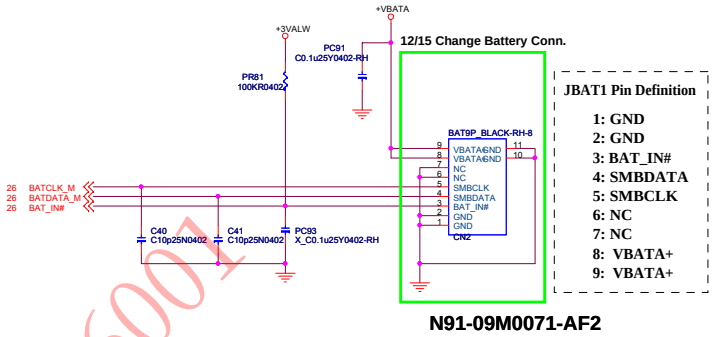
Date: Friday, October 29, 2010 | Sheet 32 of 44



MSI	MICRO-STAR INT'L CO.,LTD.		
Title	Audio Realtek ALC 269		
Size: Custom	Document Number: MS-1482	Rev: 0A	
Date: Friday, October 29, 2010	Sheet 33 of 44		

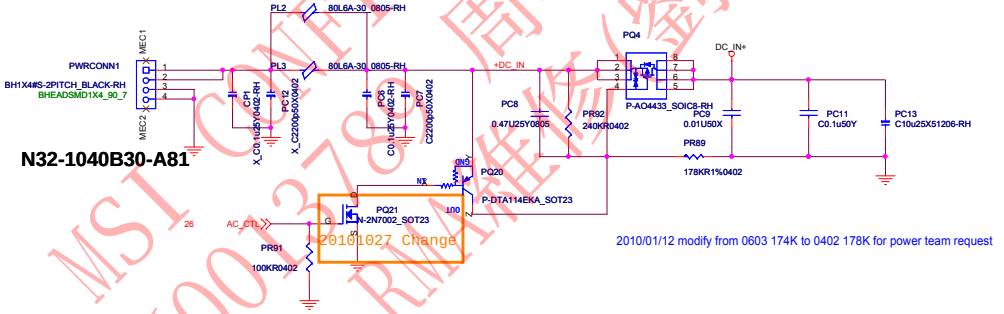
Adapter input voltage set 19 Voltage





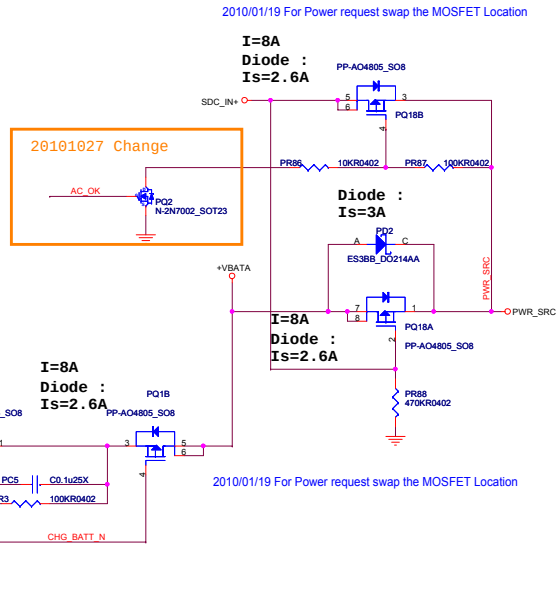
N91-09M0071-AF2

IINP :
1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
2. V_IINP = IINPUT x RS1 x 3mA/V x PR25



N32-1040B30-A81

2010/01/12 modify from 0603 174K to 0402 178K for power team request



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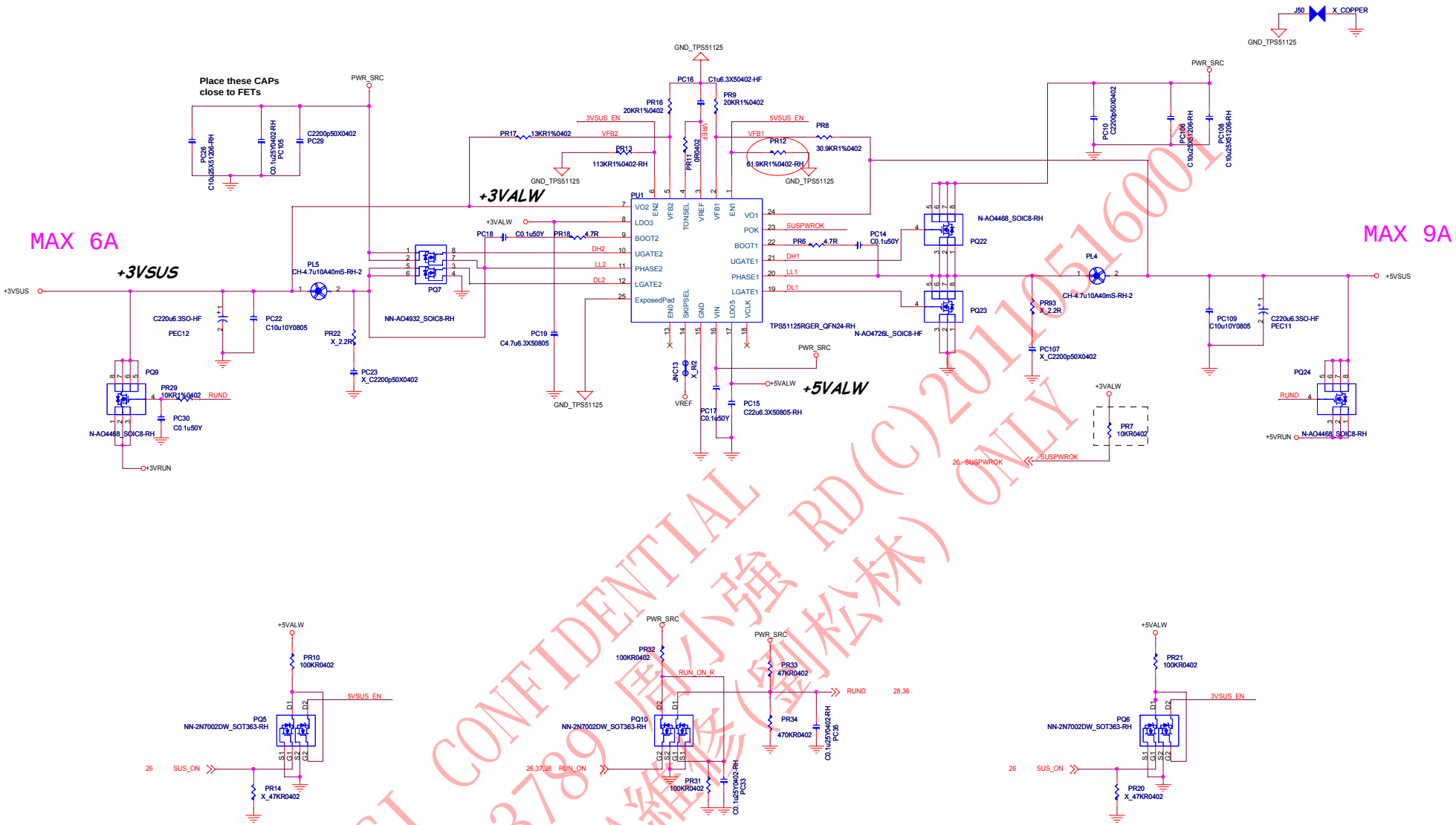
FOR RMA维修（刘松林） ONLY

MSI	MICRO-STAR INT'L CO.,LTD.		
Title	BATTERY SELETC/ CHARGER		
Size: Custom	Document Number: MS-1482		Rev: 0A
Date: Friday, October 29, 2010	Sheet 34 of 44		



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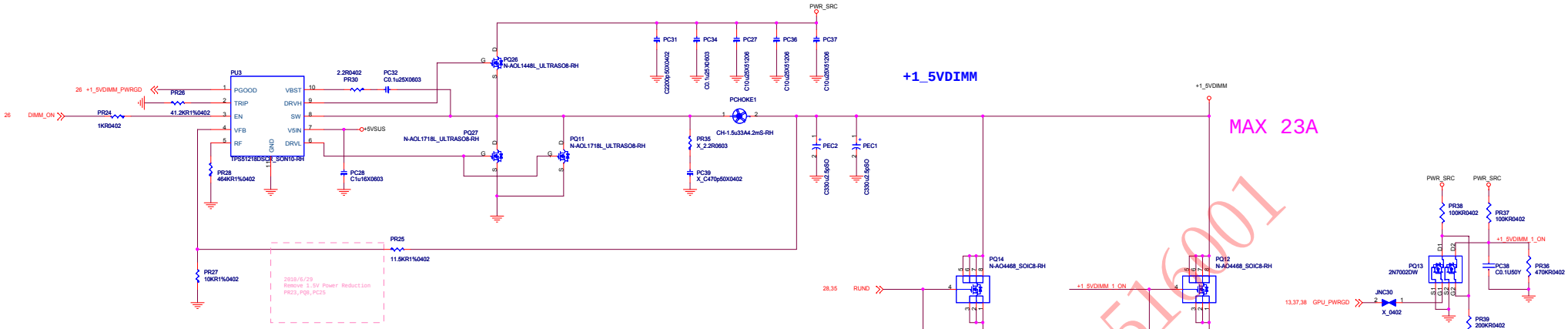
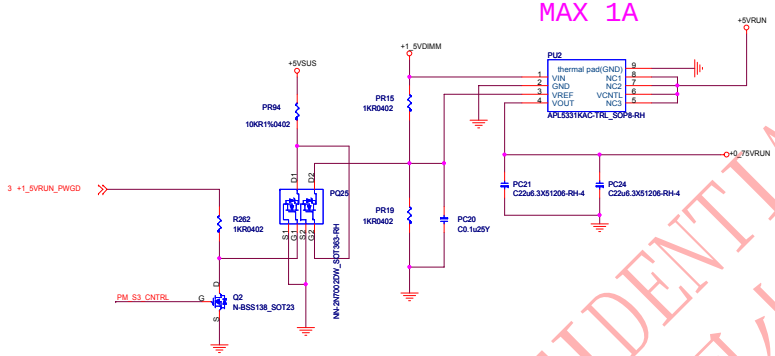
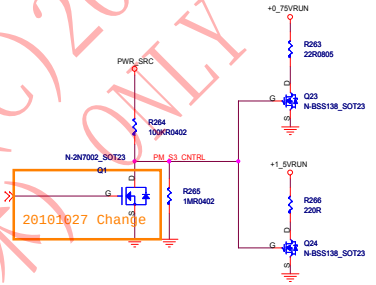
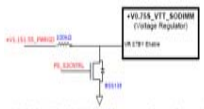
MSI	MICRO-STAR INT'L CO.,LTD.	
Title	SYSTEM POWER	
Size C	Document Number MS-1482	Rev 1.0
Date: Friday, October 29, 2010	Sheet 35 of 44	



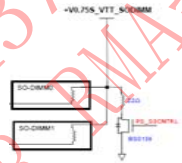




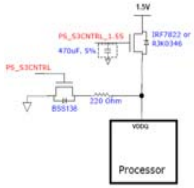


+V0.75S_VTT_DIMM should ramp up later than +V1.5S_CPU_VDDQ. Circuit shown above is used to delay +V0.75V_VTT_SODIMM ramp with respect to +V1.5S_CPU_VDDQ.

100-kΩ isolation resistor is used in reference design so that when gate is turned on, it does not pull +V1.1S1.5S_PWRGD signal to low which may impact other functionality on the board. To ensure +V1.1S1.5S_PWRGD signal levels maintained, comparator pull-up has been changed from 100 kΩ to 1 kΩ (R2F2 in Intel CRB schematic).



CKE is driven low by the processor to put the memory in self refresh while entering S3. When the processor +V1.5_CPU_VDDQ power is turned off, the discharge path on +V0.75S ensures CKE stays low during S3. To avoid any glitch on CKE signals during S3 entry, faster (22 Ω) discharge circuitry ensures +V0.75 ramps down before processor +V1.5S_CPU_VDDQ is turned off.



In current designs, Processor V_{DDQ} is powered with +V1.5, which is "ON" in S3. This is changed to a switching rail which is "OFF" during S3. A power FET is required to control the Processor V_{DDQ} (1.5 V) power. For N-FET (e.g., IRF7822 or RJK0346), gate voltage of FET (PS_S3CNTRL_1.5S) is derived from SLP_S3# and at 12-V logic. RDS(ON) of the FET used in CRB is in the range of 5 mΩ. Every design is different and designer should select an appropriate FET so that the required voltage rail specification is maintained at the Processor V_{DDQ} pins.

Signal Name	Source	Voltage Level	Comments
PS_S3CNTRL	Inverted SLP_S3# signal	In CRB, it is a 3.3-V signal.	Voltage should be high enough to turn ON or OFF the MOSFET. When selecting the MOSFET, insure $V_{th}>V_{gs}$.
PS_S3CNTRL_1.5S	Buffered SLP_S3# signal	In Intel CRB it is a 12-V signal.	Voltage should be high enough to turn ON or OFF the Power MOSFET. When selecting the MOSFET, insure $V_{th}>V_{gs}$.

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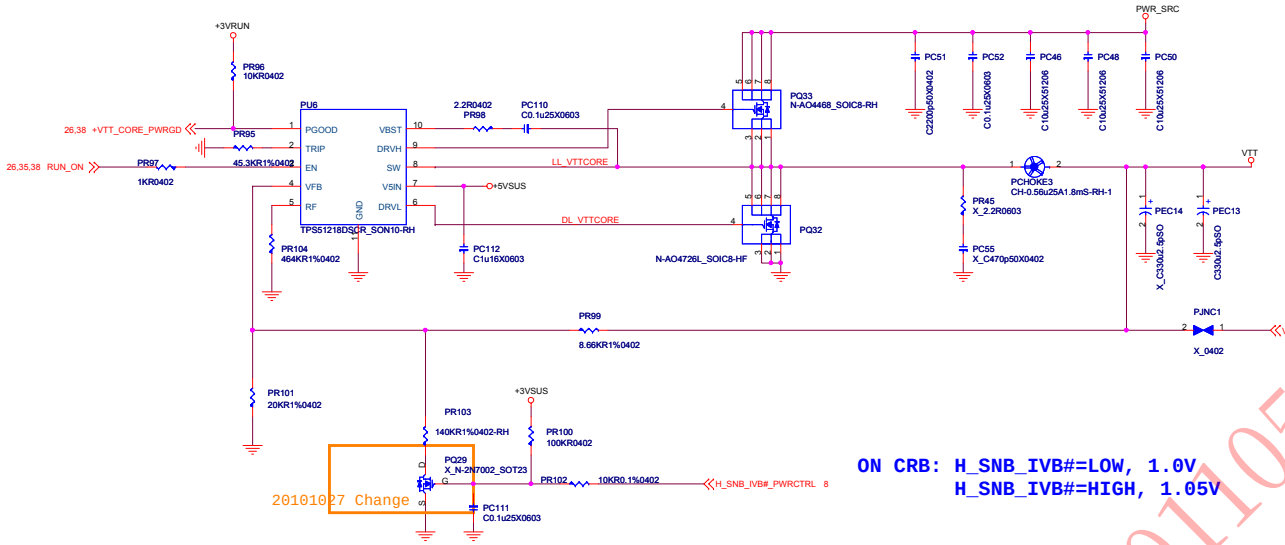
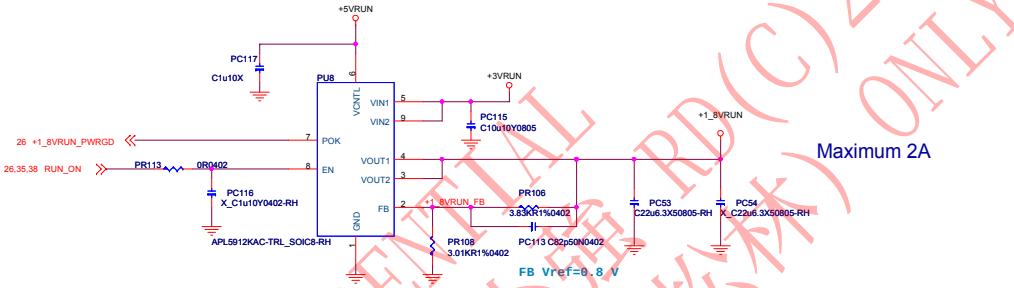
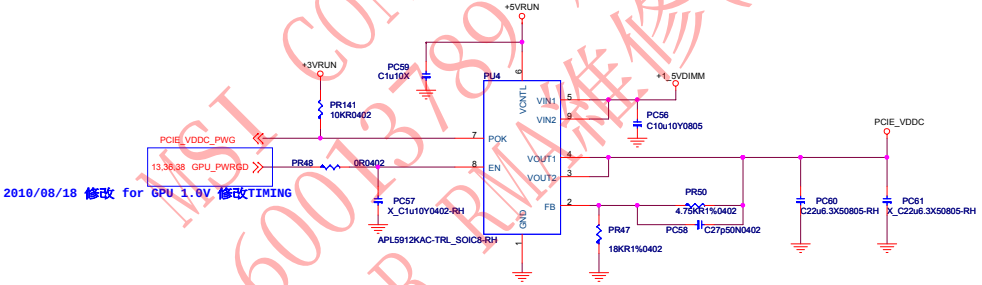
Title: SMDDR_VTERM/1_5VRUN

Size: Custom | Document Number: MS-1482 | Rev: 0A

Date: Friday, October 29, 2010 | Sheet 36 of 44







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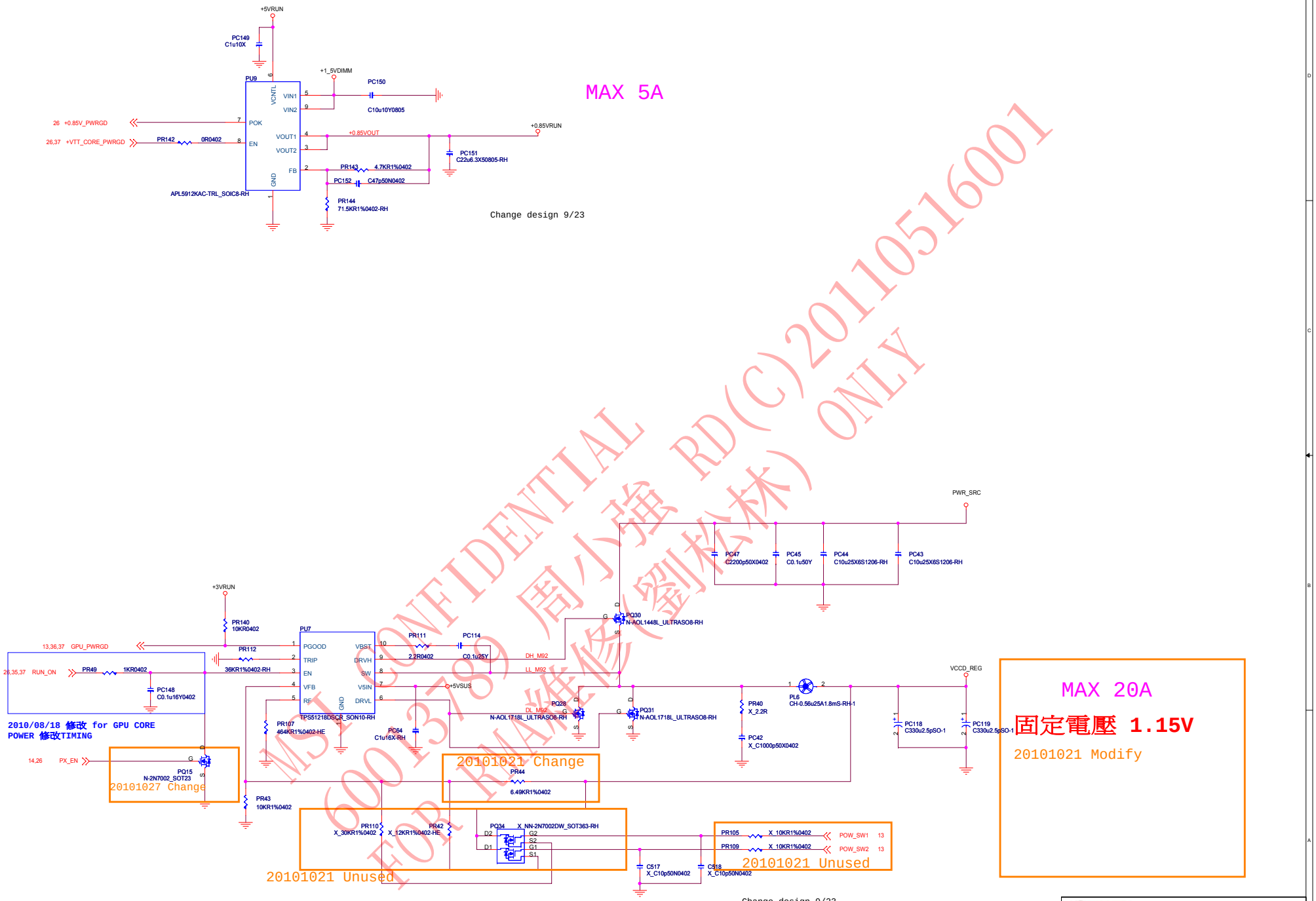
Title: VTT,+1.8VRUN,PCIE_VDDC

Size: Custom | Document Number: MS-1482 | Rev: 0A

Date: Friday, October 29, 2010 | Sheet 37 of 44



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Title: +0.85VRUN/VGA CORE

Size: C | Document Number: MS-1482 | Rev: 0A

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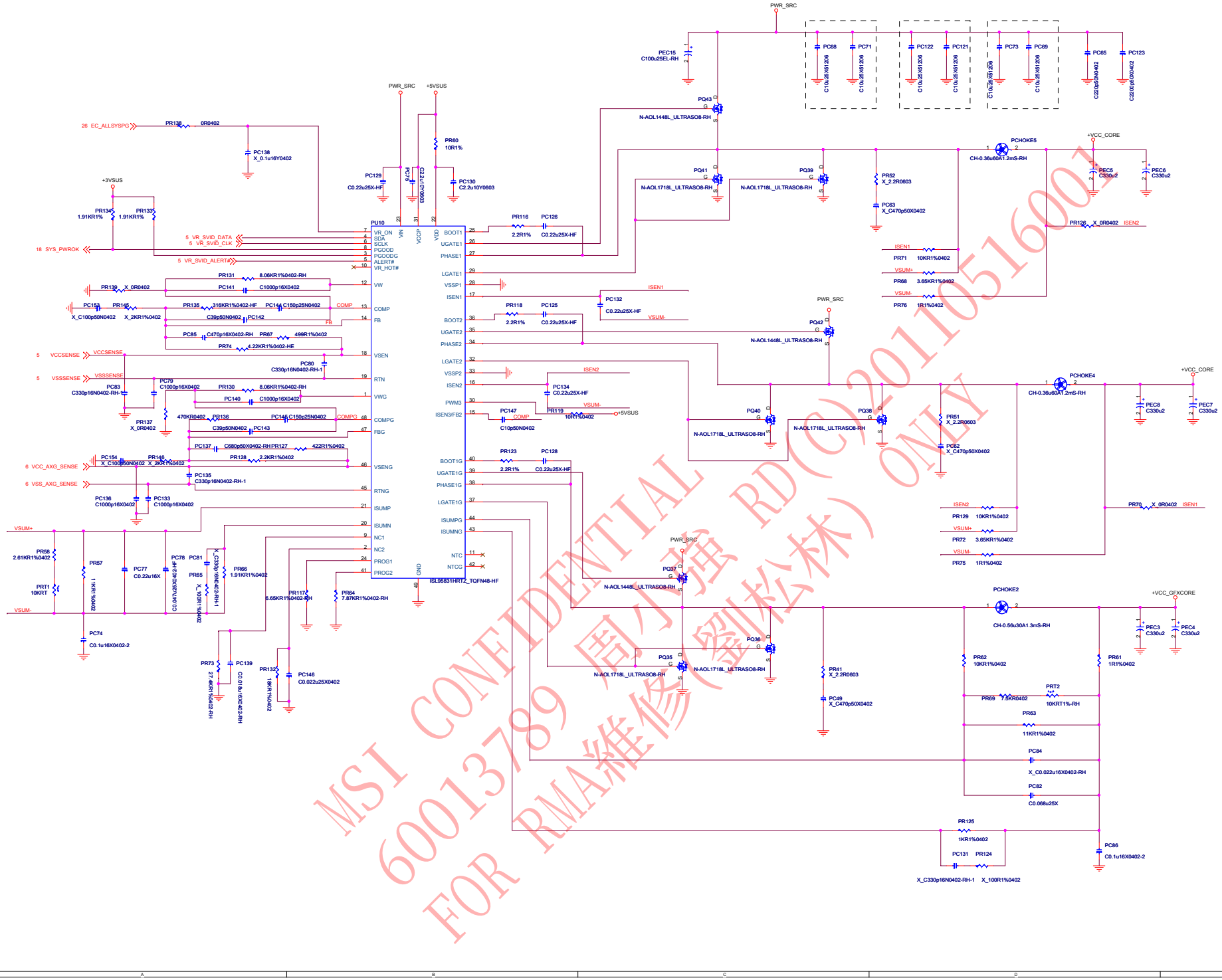

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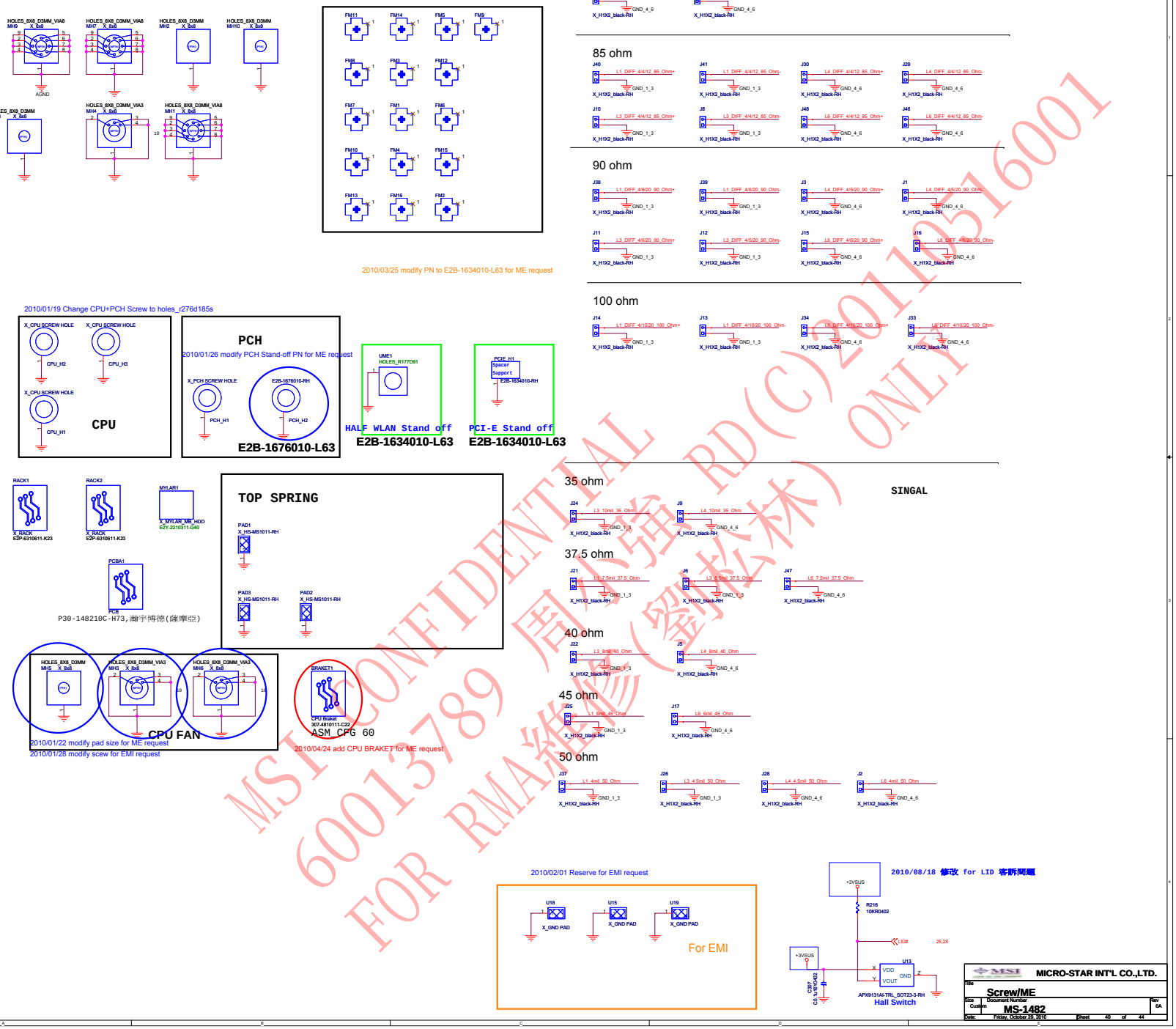
Title	CPU CORE/GCORE
Size: Custom	Document Number: MS-1482
Rev	0A
Date: Friday, October 29, 2010	Sheet 39 of 44



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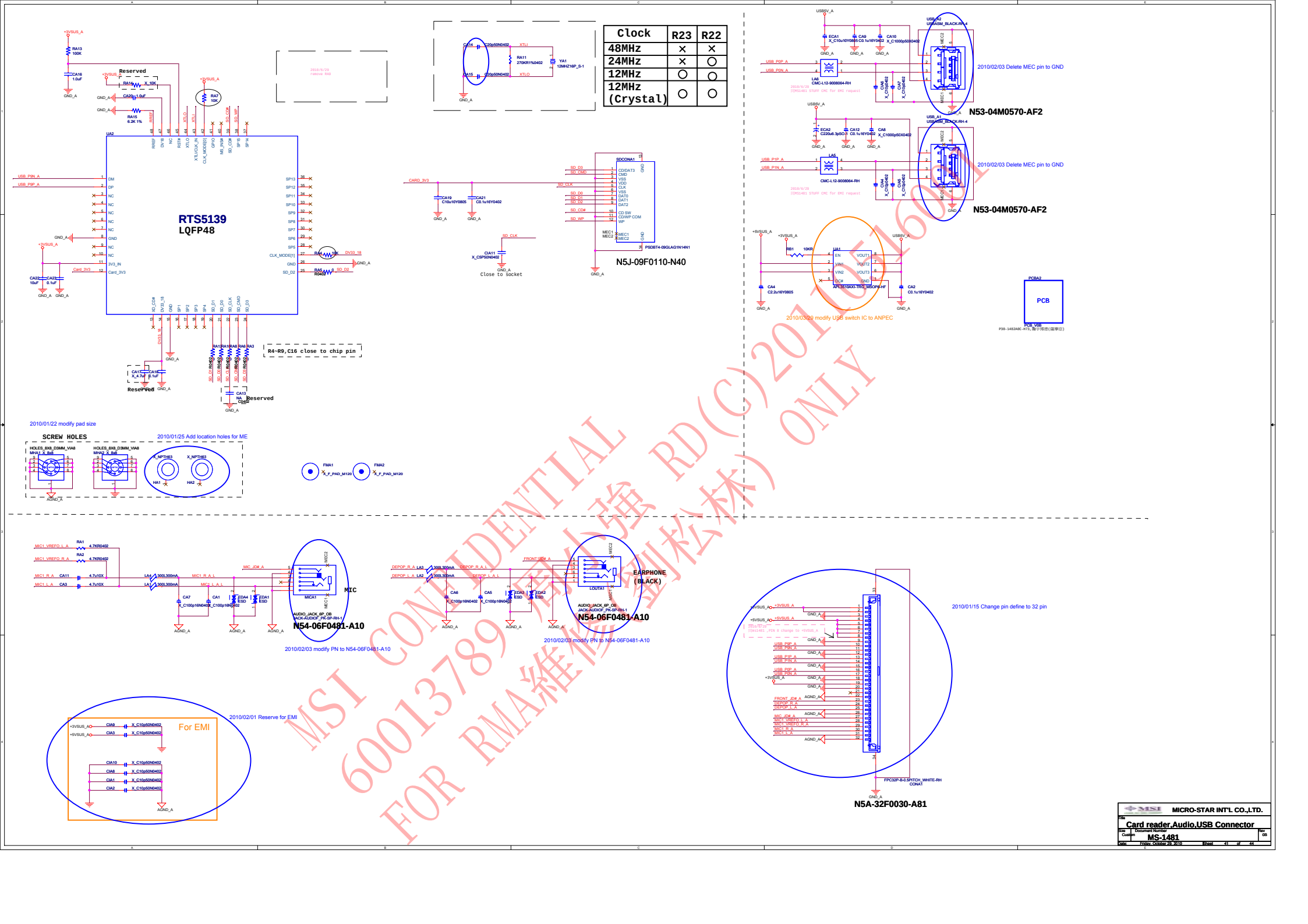

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PCBA3

PCB

PCB_V1.0

P30-1482B0C-H73,瀚宇博德(蘇摩亞)，

+3VALW_B

DB1 X_S-RB551V-30_SOD323

RB3 10KR

PWR_SW#_B

CB1 C0.1u10X0402

GND_B

FPC14P-T-0.5PITCH_WHITE-RH

CONB1

+3VALW_B
PWR_SW#_B
Cinema Pro_SW#_B
ECO_SW#_B
TURBO_SW#_B
VOL+_SW#_B
VOL-_SW#_B
LED_PWR#B
LED_ECO#B
LED_TURBO#B
LED_Cinema Pro#_B
TPJNC_B4
TPJNC_B5
+5VRUN_B

N5A-14F0090-A81

VOL+_SW#_B JNCB6 X_0402 SWB3 SW-TACT-1B CIB6 X_C0.1u16Y0402

N71-0101630-D02

VOL-_SW#_B JNCB4 X_0402 SWB4 SW-TACT-1B CIB4 X_C0.1u16Y0402

N71-0101630-D02

TURBO_SW#_B JNCB5 X_0402 SWB5 SW-TACT-1B CIB5 X_C0.1u16Y0402

N71-0101630-D02

Cinema Pro_SW#_B JNCB2 X_0402 SWB1 SW-TACT-1B CIB1 X_C0.1u16Y0402

N71-0101630-D02

ECO_SW#_B JNCB3 X_0402 SWB6 SW-TACT-1B CIB3 X_C0.1u16Y0402

N71-0101630-D02

PWR_SW#_B JNCB1 X_0402 SWB2 SW-TACT-1B CIB2 X_C0.1u16Y0402

N71-0101630-D02

LED

+5VRUN_B

RNB1 8P4R-220R0402

DB5 LED04-B-20mA3.8V_3216-RH

DB6 LED04-O-30mA2.0V_320160-HF

LED_PWR#B BLUE

LED_TURBO#B ORANGE

D0C-0405230-L05

D0C-0409300-L05

FMB3 X_F_PAD_M120

FMB2 X_F_PAD_M120

FMB1 X_F_PAD_M120

FMB4 X_F_PAD_M120

MYLARB1

MYLAR_Launch

E2P-4811711-Y42

SCREW HOLES

MHB1 X_R6.2D2.7 holes_r244d106

MHB2 X_R6.2D2.7 holes_r244d106

X_NPTH63

X_NPTH63

HB1

HB2

GND_B

For EMI

LED_PWR#B CIB8 X_C100p16N0402

LED_ECO#B CIB9 X_C100p16N0402

LED_TURBO#B CIB10 X_C100p16N0402

LED_Cinema Pro#_B CIB7 X_C100p16N0402

+5VRUN_B CIB11 X_C100p16N0402

GND_B

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Title: Launch Board

Size: Custom | Document Number: MS-1481 | Rev: 1.0

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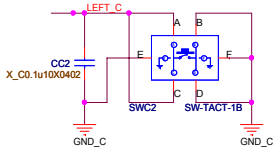

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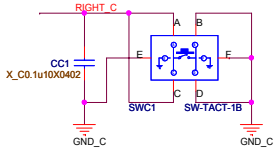

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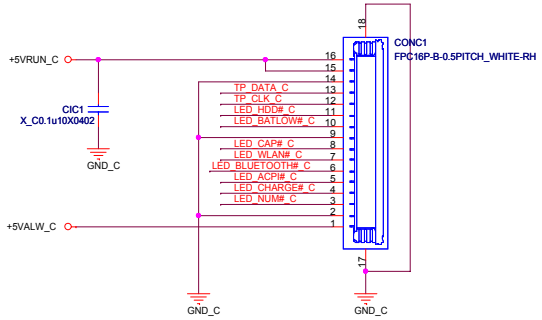

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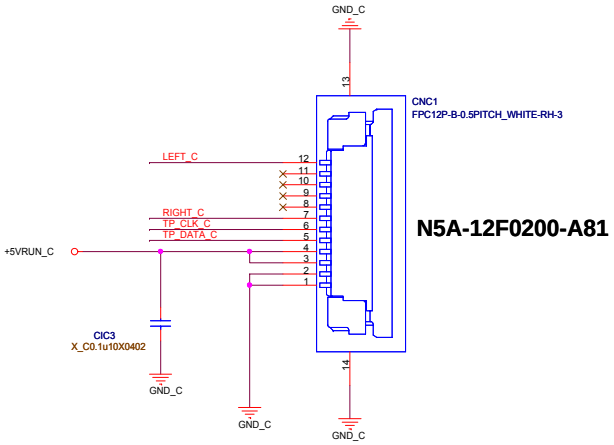

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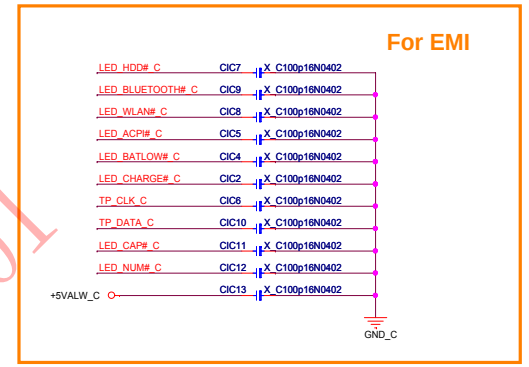
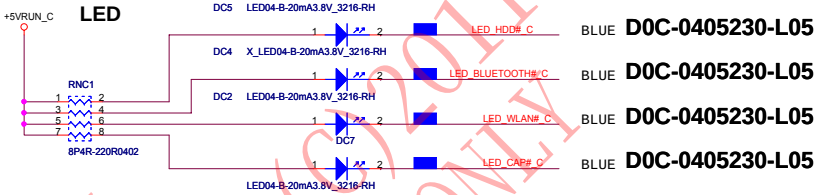
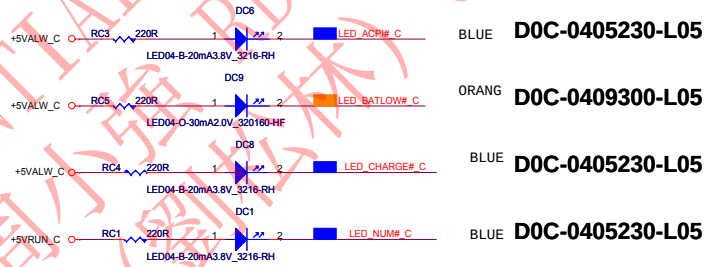


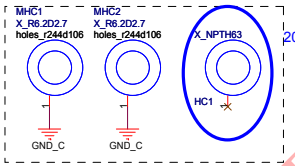




E2P-4811811-Y42

P30-1482C0C-H73,瀚宇博德(蘇摩亞)

SCREW HOLES



2010/01/25 Add location holes for ME

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Title: TP,LEDBOARD

Size: Custom | Document Number: MS-1481 | Rev: 1.0

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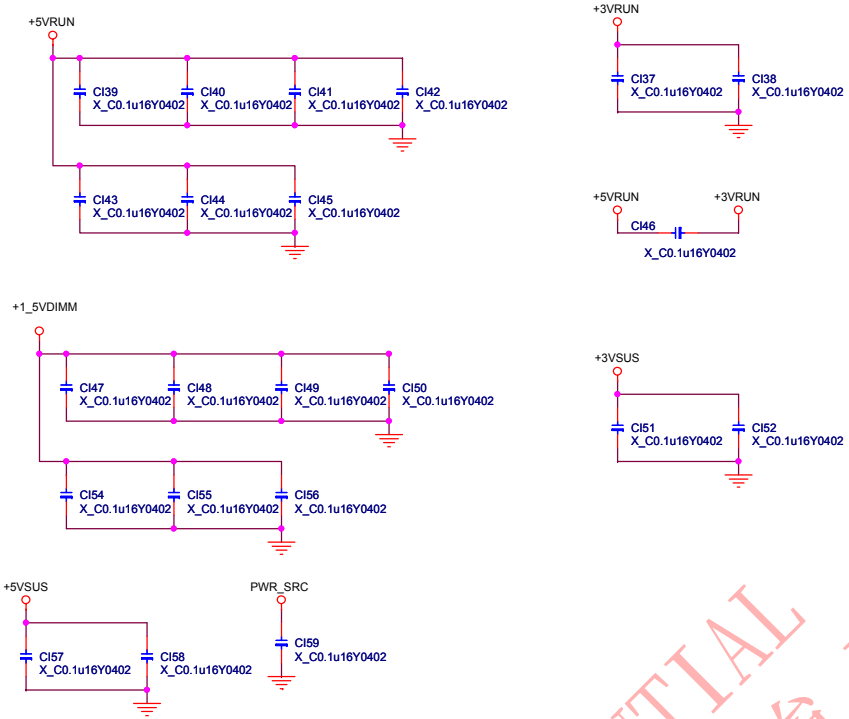

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Size A3	Document Number <Doc>	Rev <RevCode>
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